LatticeECP2/M Family Data Sheet

DS1006 Version 02.7, July 2007

LatticeECP2/M Family Data Sheet Introduction

July 2007 Advance Data Sheet DS1006

Features

- **High Logic Density for System Integration**
  - 6K to 95K LUTs
  - 90 to 616 I/Os
- **Embedded SERDES (LatticeECP2M Only)**
  - Data Rates 540 Mbps to 3.125 Gbps
  - 270 Mbps with Half Rate mode
    Up to 16 channels per device
    PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.
- **sysDSP™ Block**
  - 3 to 42 blocks for high performance multiply and accumulate
  - Each block supports
    - One 36x36, four 18X18 or eight 9X9 multipliers
- **Flexible Memory Resources**
  - 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
    - 18Kbit block
    - Single, pseudo dual and true dual port
    - Byte Enable Mode support
  - 12K to 202Kbits distributed RAM
    - Single port and pseudo dual port
- **sysCLOCK Analog PLLs and DLLs**
  - Two GPLLs and up to six SPLLs per device
    - Clock multiply, divide, phase & delay adjust
    - Dynamic PLL adjustment
  - Two general purpose DLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - Source synchronous standards support
    - SPI4.2, SFI4 (DDR Mode), XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR and DDR2 memory support
    - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
  - Dedicated DQS support
- **Programmable sysIO™ Buffer Supports Wide Range Of Interfaces**
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 3/2/18 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL
- **Flexible Device Configuration**
  - 1149.1 Boundary Scan compliant
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual boot images supported
  - TransFR™ I/O for simple field updates
  - Soft Error Detect macro embedded
- **Optional Bitstream Encryption (LatticeECP2/M "S" Versions Only)**
- **System Level Support**
  - ispTRACY™ internal logic analyzer capability
  - On-chip oscillator for initialization & general use
  - 1.2V power supply

Table 1-1. LatticeECP2 (including "S-Series") Family Selection Guide

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	56
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	

Table 1-1. LatticeECP2 (including "S-Series") Family Selection Guide

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

Table 1-2. LatticeECP2M (including "S-Series") Family Selection Guide

Device	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL+SPLL+DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	430	616
Packages and SERDES / I/O Combinations					
256-ball fpBGA (17 x 17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23 x 23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27 x 27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31 x 31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35 x 35 mm)				16 / 430	16 / 520
1156-ball fpBGA (35 x 35 mm)					16 / 616

Introduction

The LatticeECP2/M family of FPGA devices has been optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M family of devices features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP2/M family of FPGA devices. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP2/M family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP2/M Family Data Sheet Architecture

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Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing blocks as shown in the ECP2-6 in Figure 2-1. In addition, the LatticeECP2M family contain SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer). Each SERDES Channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES along with its Physical Coding Sub-layer (PCS) block creates a Quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeECP2/M devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of the high speed source synchronous standards such as SPI4.2 along with memory interfaces including DDR2.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. Every device in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP2/M devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, ECP2-6 Device (Top Level)

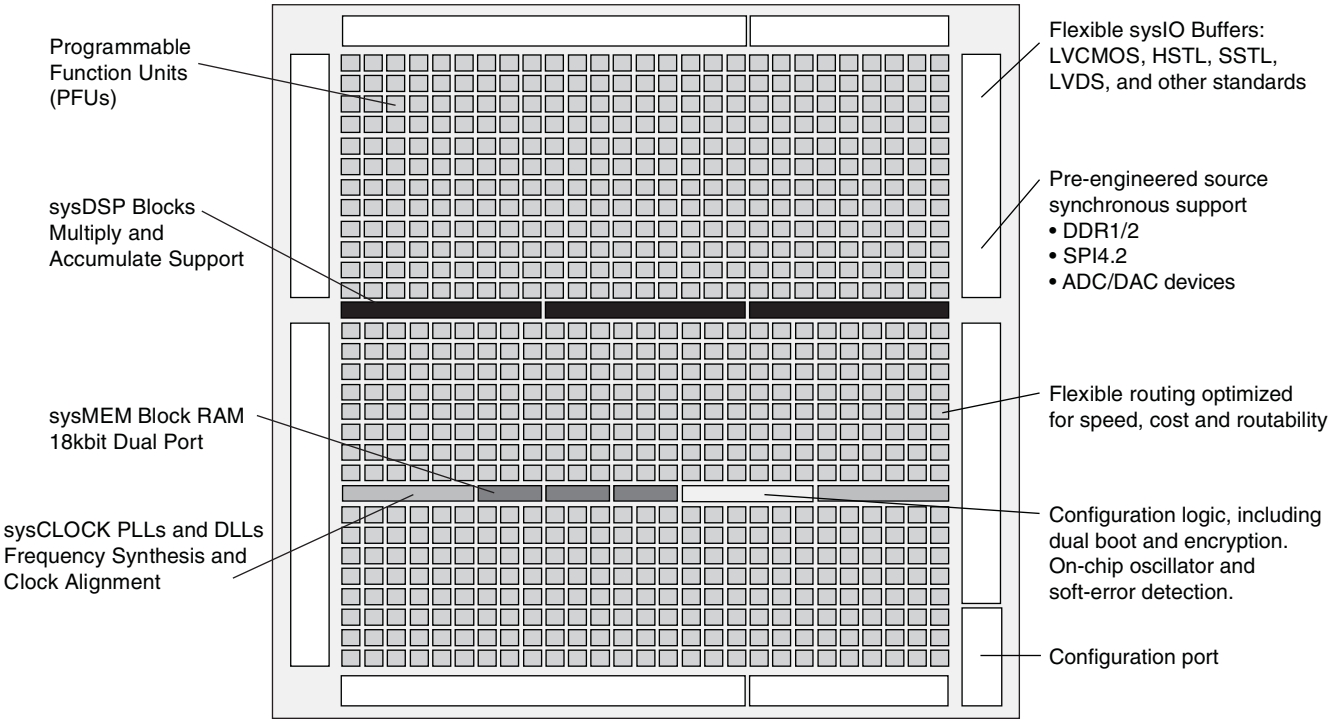
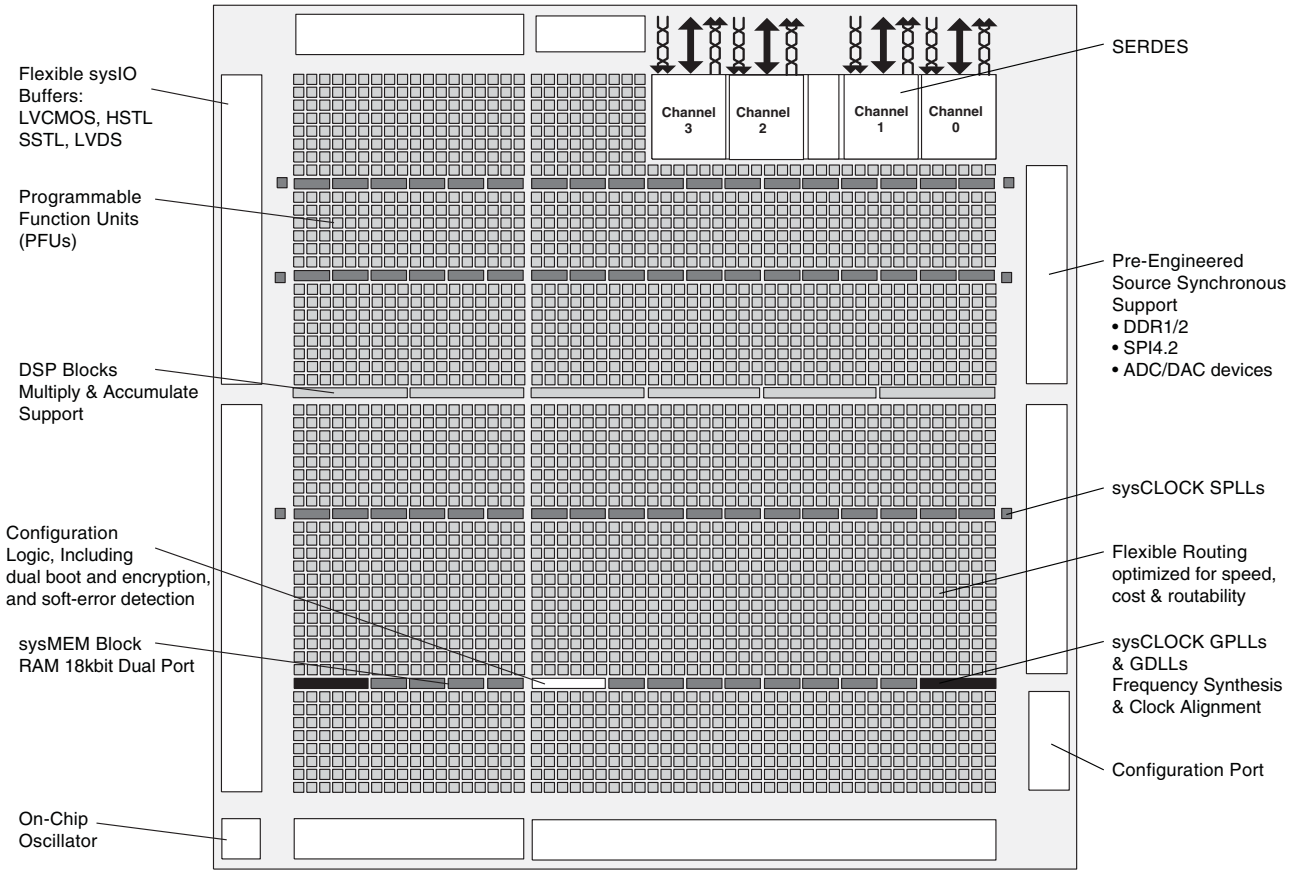


Figure 2-2. Simplified Block Diagram, ECP2M20 Device (Top Level)

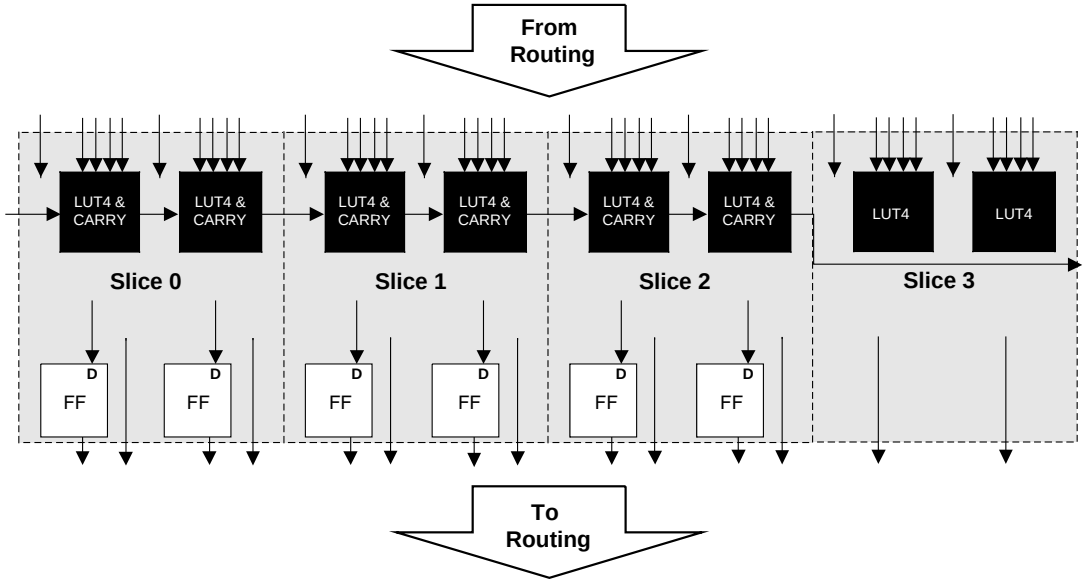


PFU Blocks

The core of the LatticeECP2/M device consists of PFU blocks which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

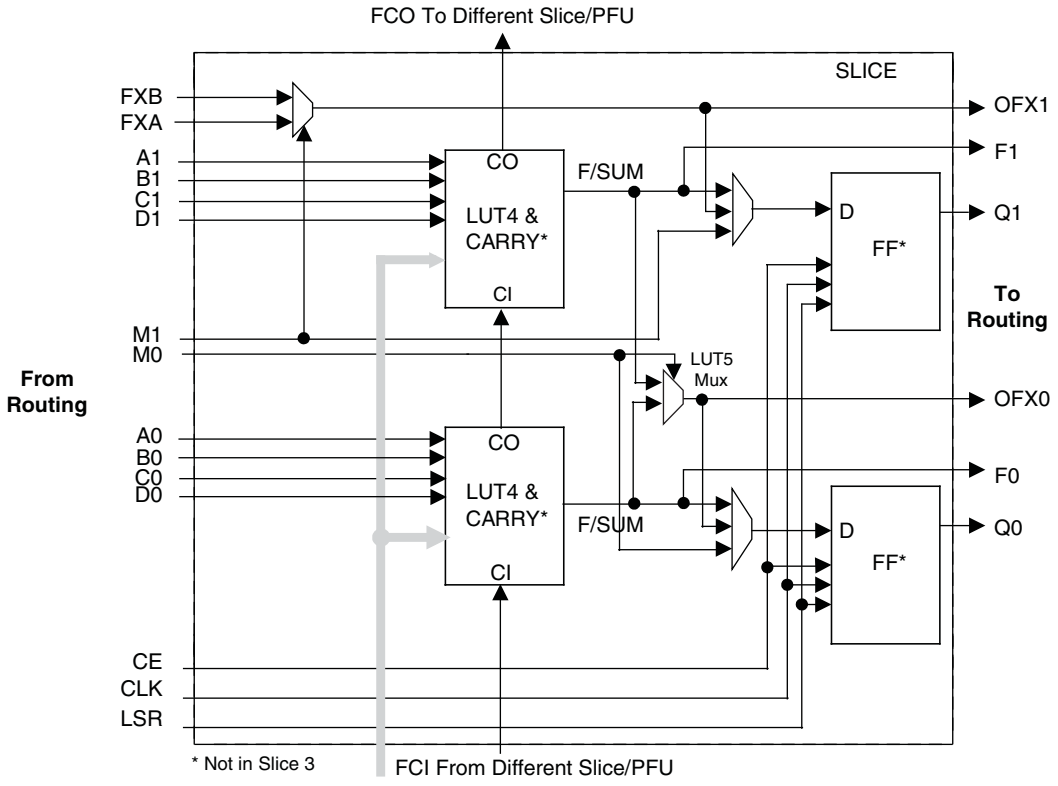
Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains some logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Figure 2-4. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode
Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode
In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeECP2/M devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeECP2/M devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The LatticeECP2/M family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (GPLL/SPLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP2/M family support two General Purpose PLLs (GPLLs) which are full-featured PLLs. In addition, some of the larger devices have two to six Standard PLLs (SPLLs) that have a subset of GPLL functionality.

General Purpose PLL (GPLL)

The architecture of the GPLL is shown in Figure 2-5. A description of the GPLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP or from a user clock PIN/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

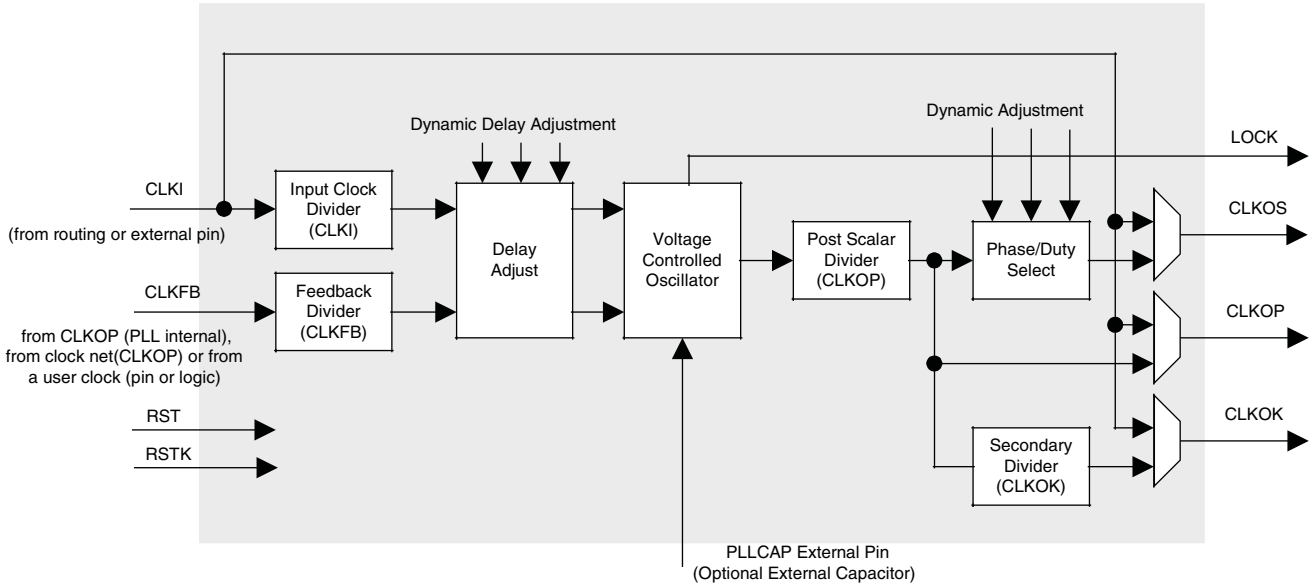
The Delay Adjust Block adjusts either the delays of the reference or feedback signals. The Delay Adjust Block can either be programmed during configuration or can be adjusted dynamically. The setup, hold or clock-to-out times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock.

Following the Delay Adjust Block, both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied. LatticeECP2/M devices have two dedicated pins on the left and right edges of the device for connecting optional external capacitors to the VCO. This allows the PLLs to operate at a lower frequency. This is a shared resource which can only be used by one PLL (GPLL or SPLL) per side.

The output of the VCO then enters the post-scalar divider. The post-scalar divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. A secondary divider takes the CLKOP signal and uses it to derive lower frequency outputs (CLKOK). The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOP signal and generates the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The primary output from the post scalar divider CLKOP along with the outputs from the secondary divider (CLKOK) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

Figure 2-5. General Purpose PLL (GPLL) Diagram



Standard PLL (SPLL)

Some of the larger devices have two to six Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see details of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

Table 2-4. GPLL and SPLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE[1]	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR[1]	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG[1]	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0][1]	I	Dynamic Delay Input
DPA MODES	I	DPA (Dynamic Phase Adjust/Duty Cycle Select) mode
DPHASE [3:0]	I	DPA Phase Adjust inputs
DDDUTY [3:0]	—	DPA Duty Cycle Select inputs

1. These signals are not available in SPLL.

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2/M family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is feed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLLDELA delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-6 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information on the DLL, please see details of additional technical documentation at the end of this data sheet.

Figure 2-6. Delay Locked Loop Diagram (DLL)

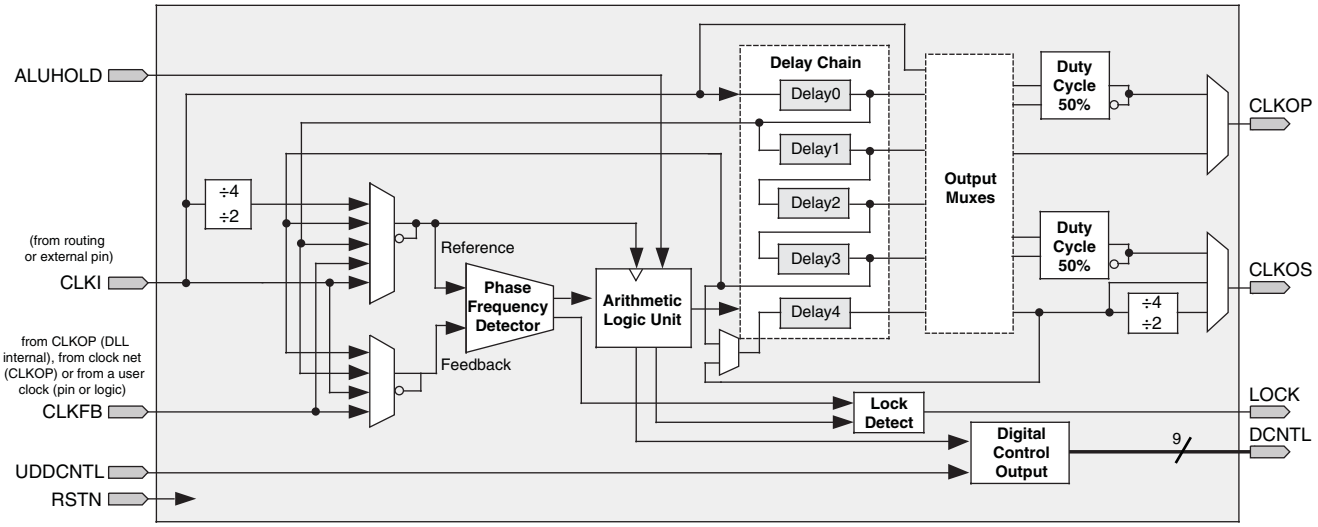


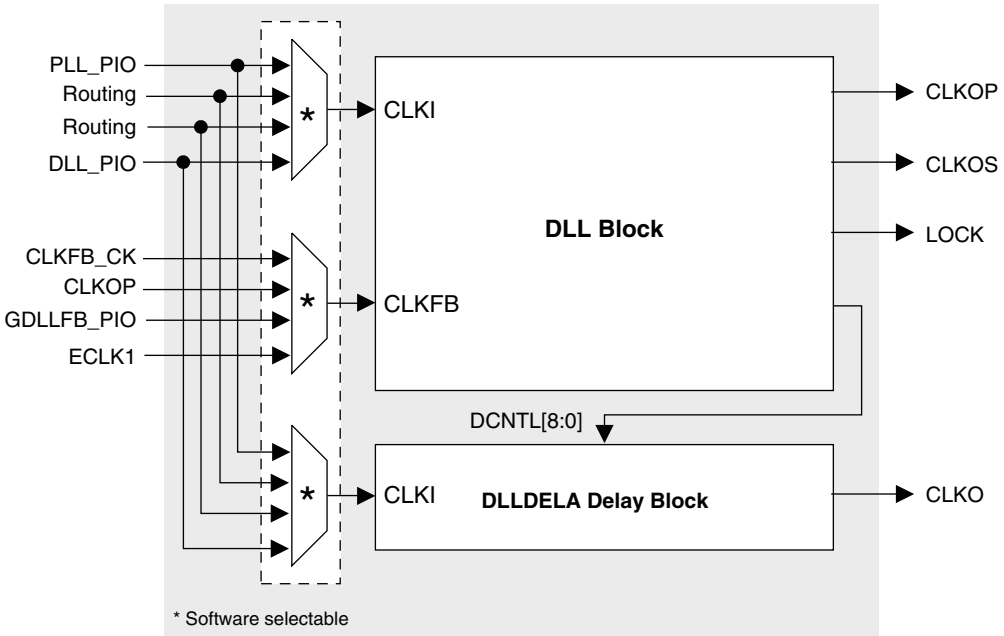
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see details of additional technical documentation at the end of this data sheet.

Figure 2-7. DLLDELA Delay Block



PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are as follows:

- PLL to PLL supported
- PLL to DLL supported

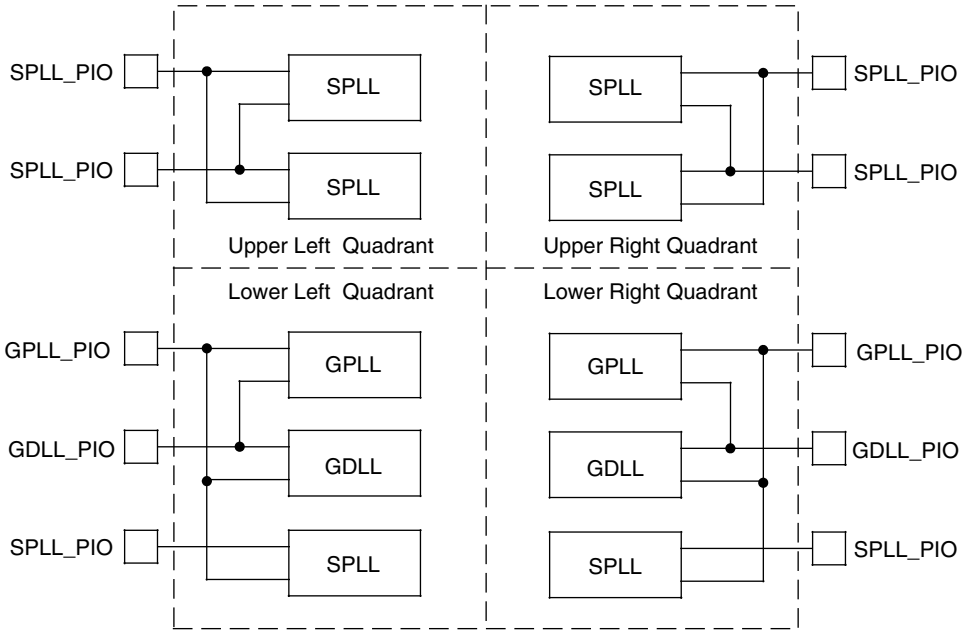
The DLLs in the LatticeECP2/M are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

GPLL/SPLL/GDLL PIO Input Pin Connections (LatticeECP2M Family Only)

All LatticeECP2M devices contain two GDLLs, two GPLLs and six SPLLs, arranged in quadrants as shown in Figure 2-8. In the LatticeECP2M devices GPLLs, SPLLs and GDLLs share their input pins. Figure 2-8 shows the sharing of SPLLs input pin connections in the upper two quadrants and the sharing of GDLL, GPLL and SPLL input pin connections in the lower two quadrants.

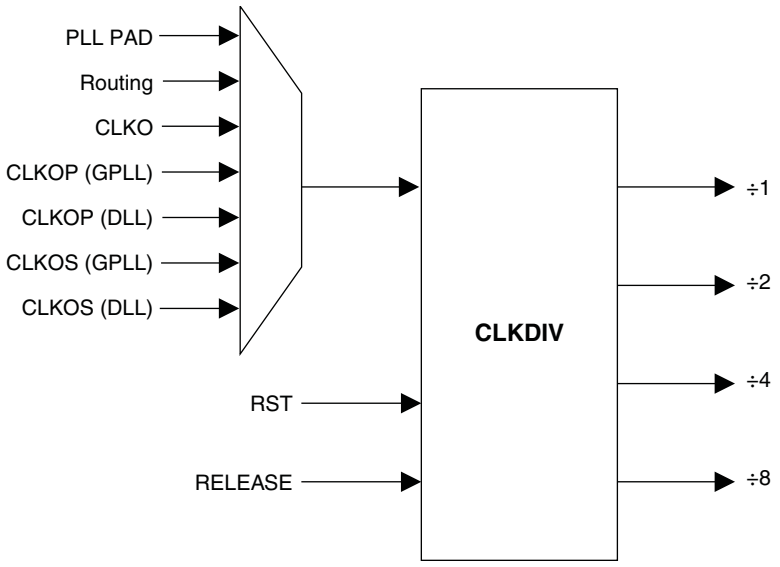
Figure 2-8. Sharing of PIO Pins by GPLL, SPLL and GDLL in LatticeECP2M Devices



Clock Dividers

LatticeECP2/M devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL-DELA delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see details of additional technical documentation at the end of this data sheet. Figure 2-9 shows the clock divider connections.

Figure 2-9. Clock Divider Connections



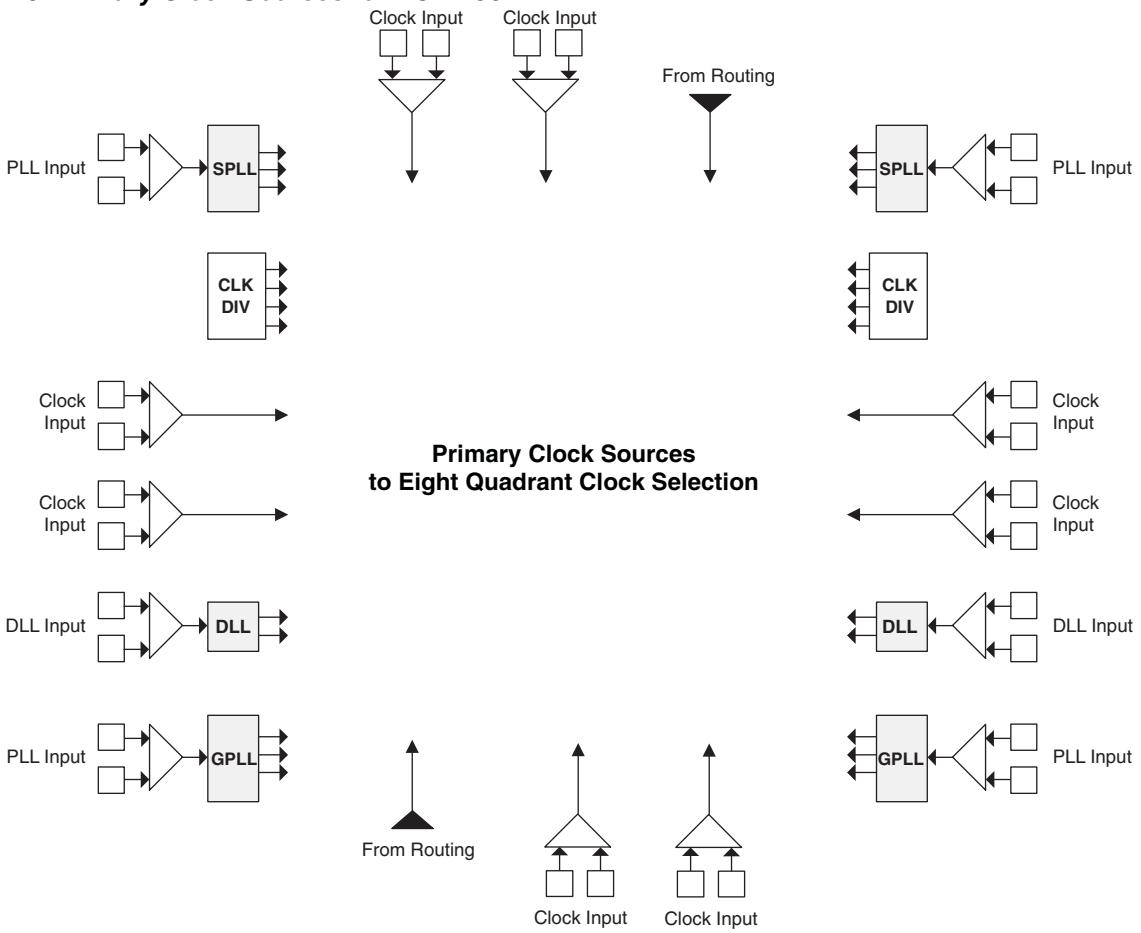
Clock Distribution Network

LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

Figure 2-10. Primary Clock Sources for ECP2-50

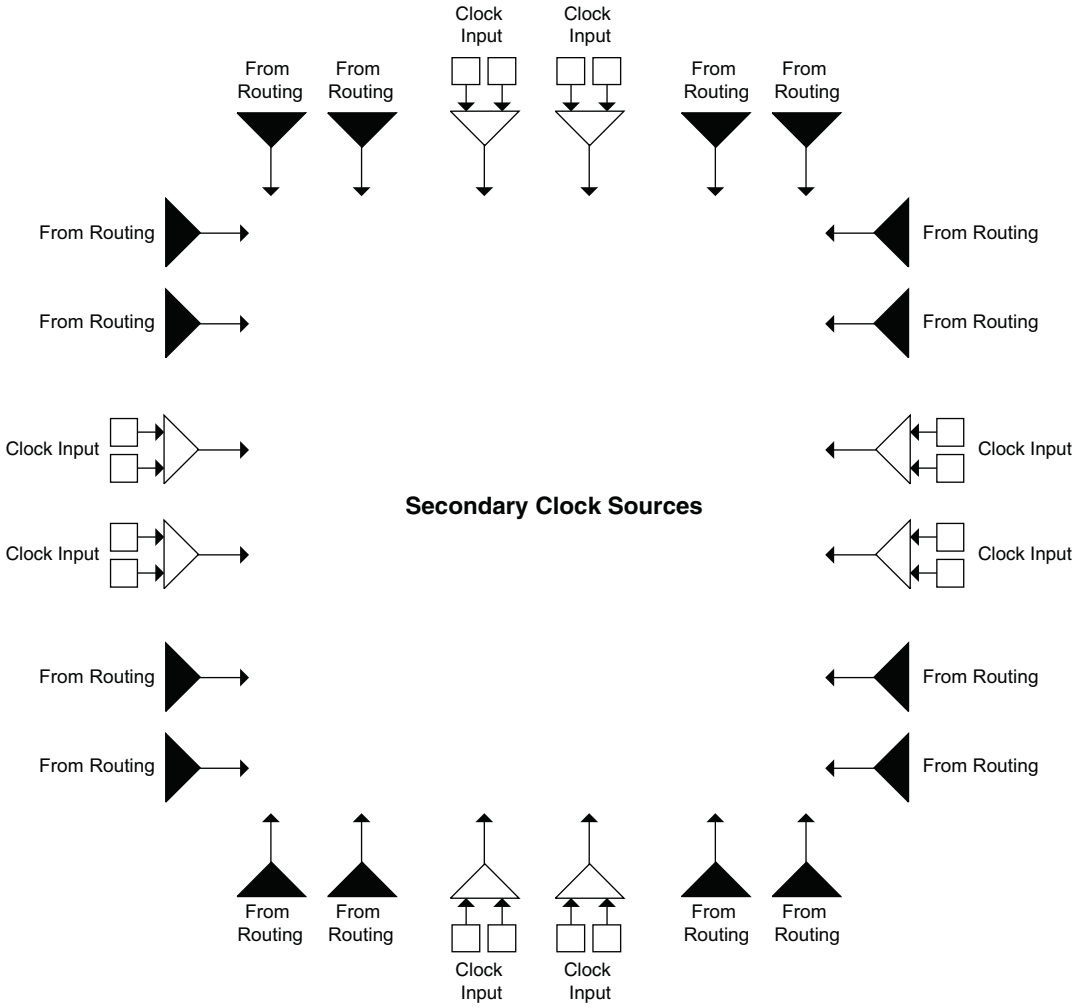


Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M device have six SPLLs.

Secondary Clock/Control Sources

LatticeECP2/M devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-11 shows the secondary clock sources.

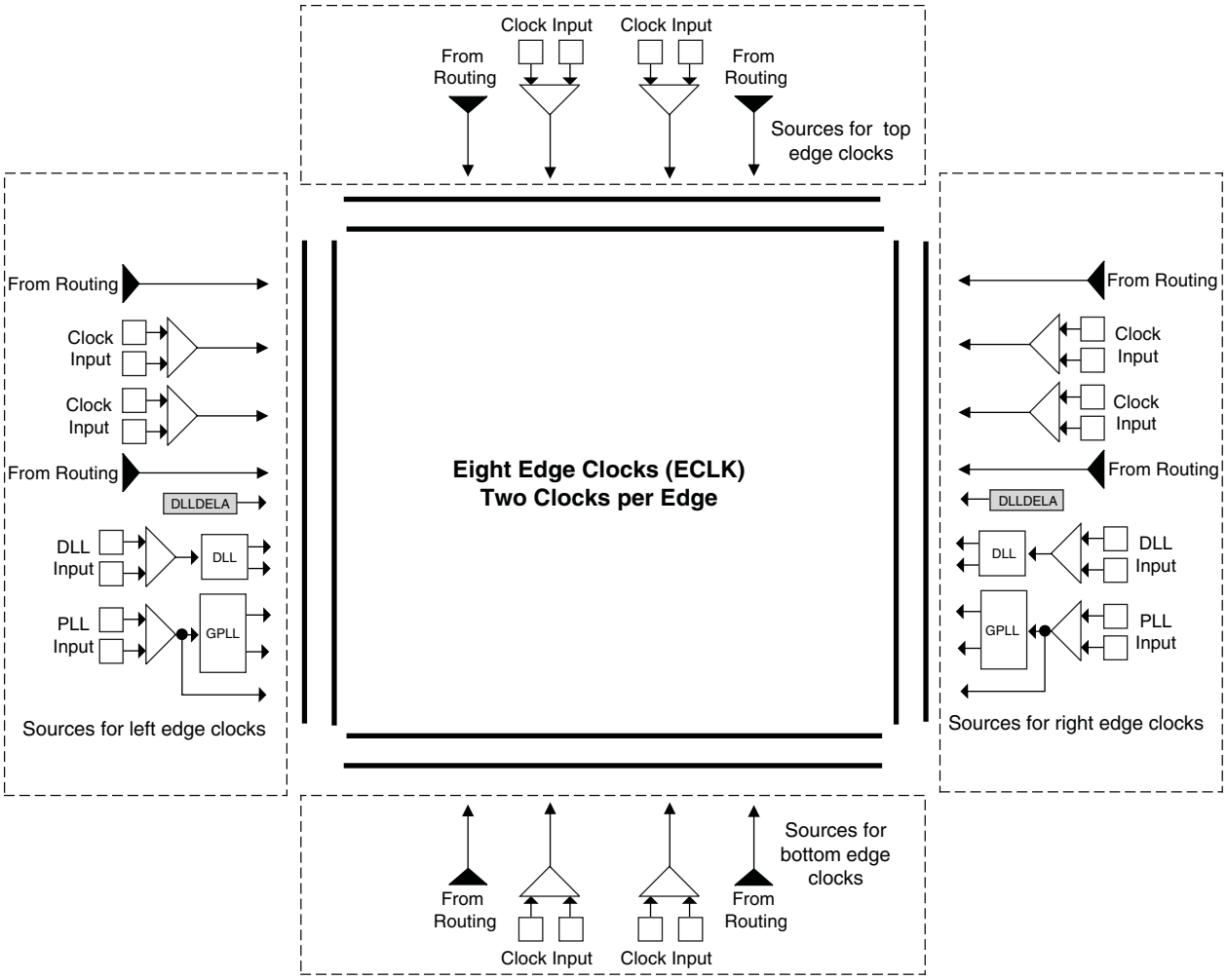
Figure 2-11. Secondary Clock Sources



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

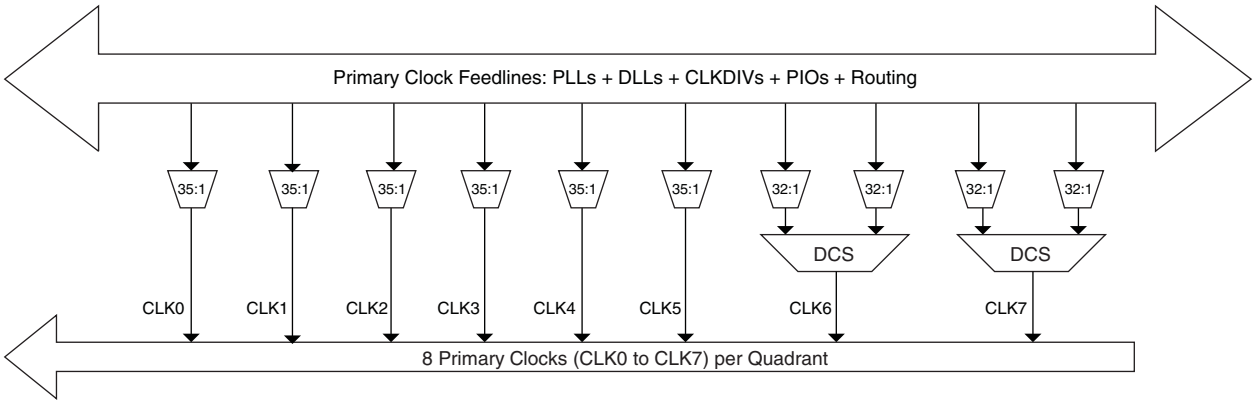
Figure 2-12. Edge Clock Sources



Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

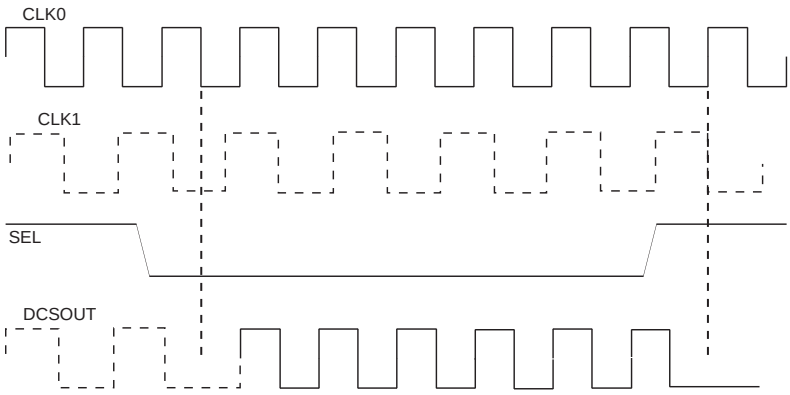


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have eight secondary clock and control signal resources per region (SC0 to SC7).

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing.

Figure 2-15. Secondary Clock Regions ECP2-50

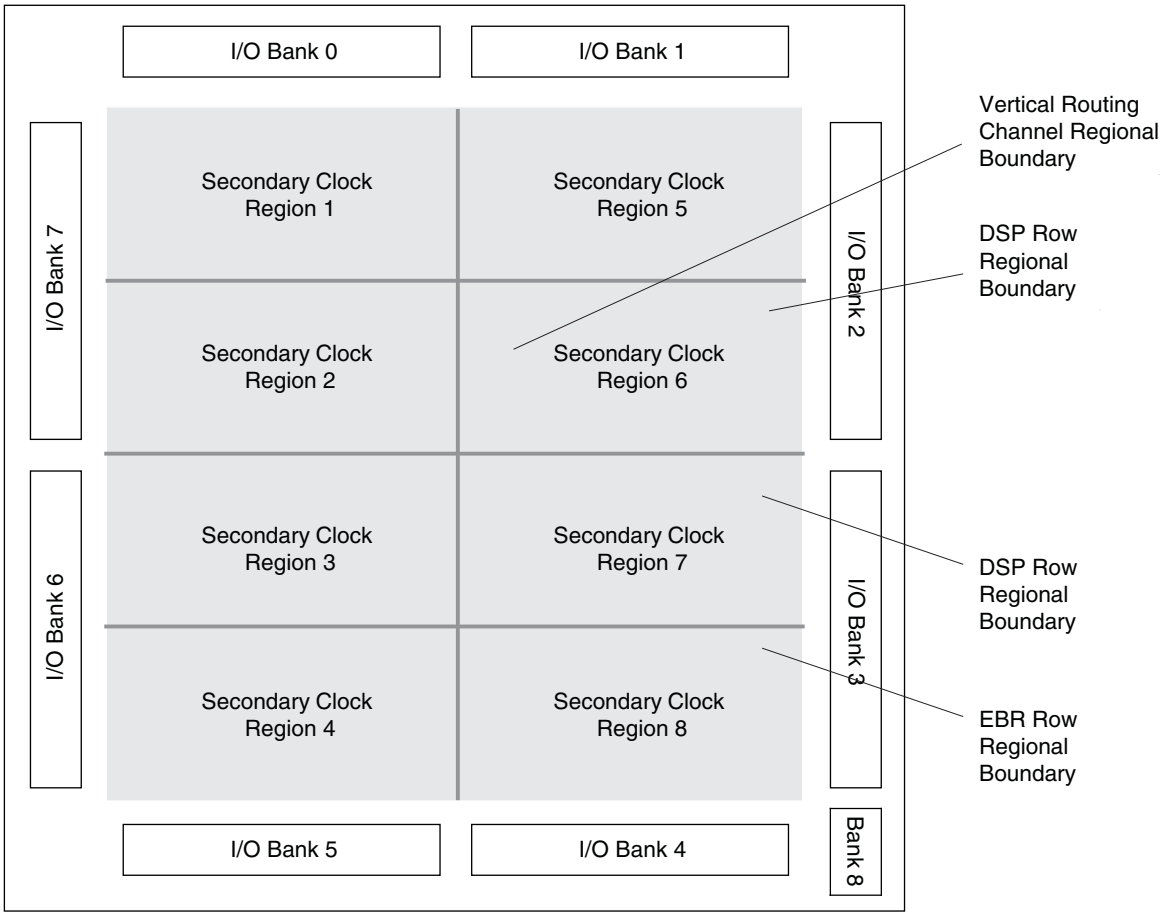
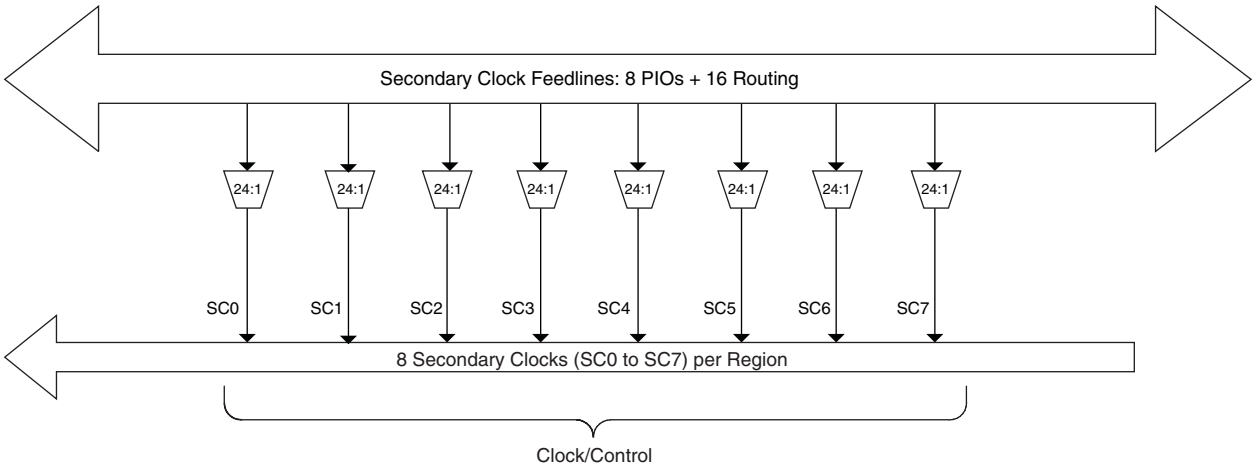


Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals via routing can be used as a clock input to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

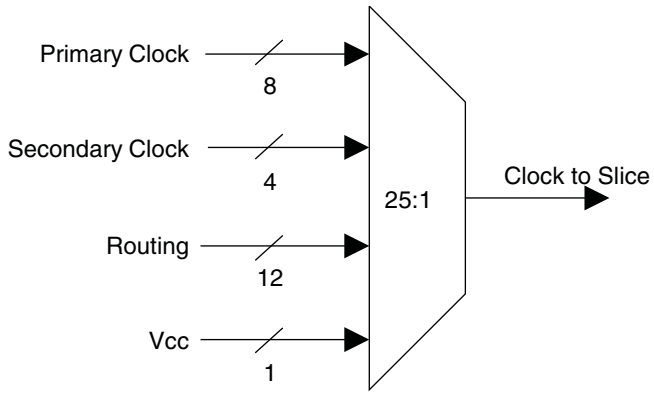
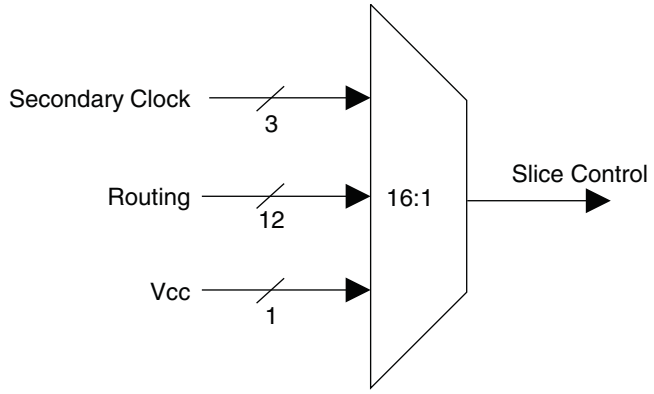


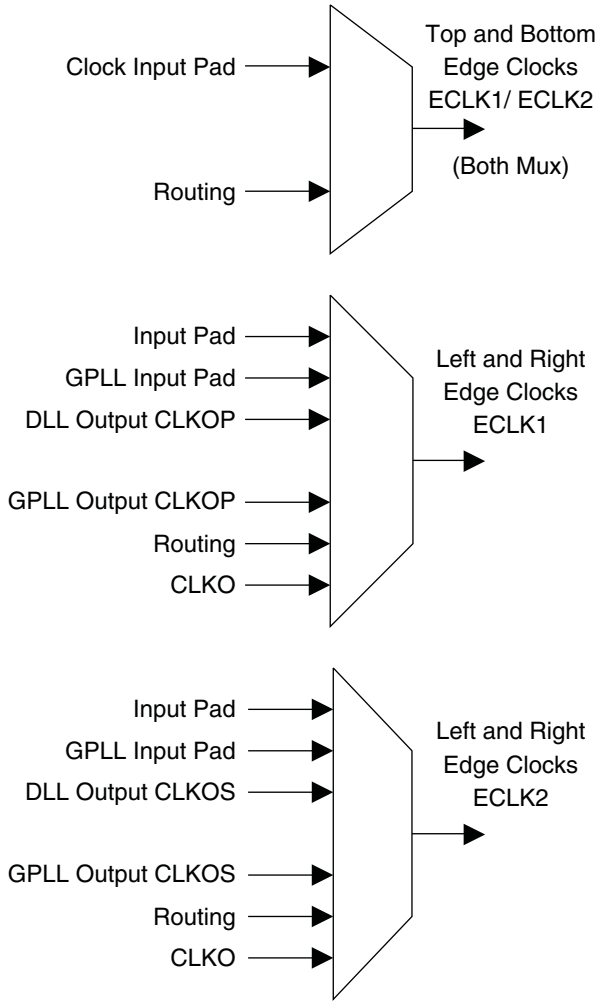
Figure 2-18. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeECP2/M devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per device: two edge clocks per edge. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKO signal (generated from the DLLDELA block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-19 shows the selection muxes for these clocks.

Figure 2-19. Edge Clock Mux Connections



sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports three forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

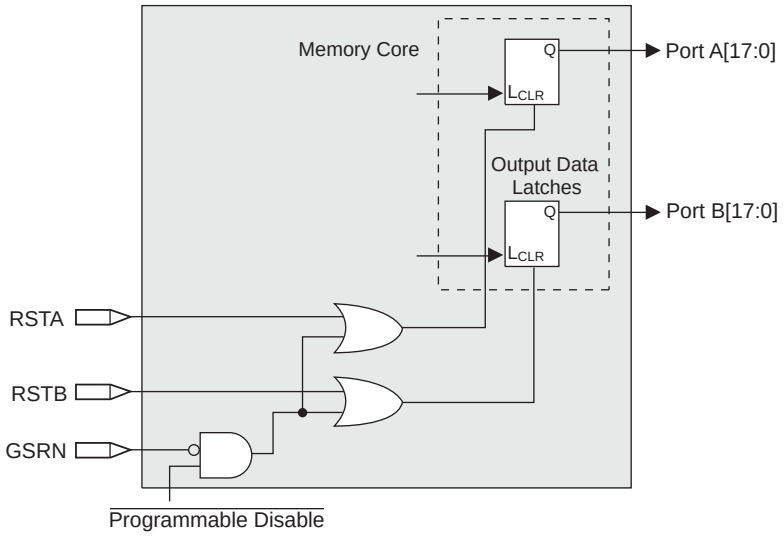
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

3. Read-Before-Write – When new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

Figure 2-20. Memory Core Reset

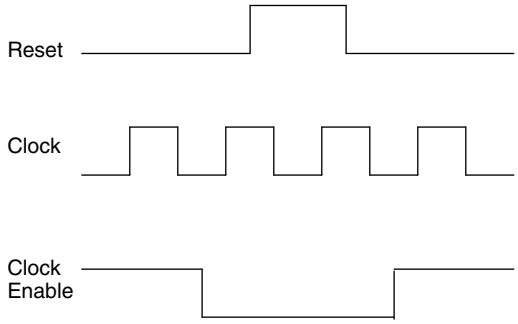


For further information on the sysMEM EBR block, please see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP™ Block

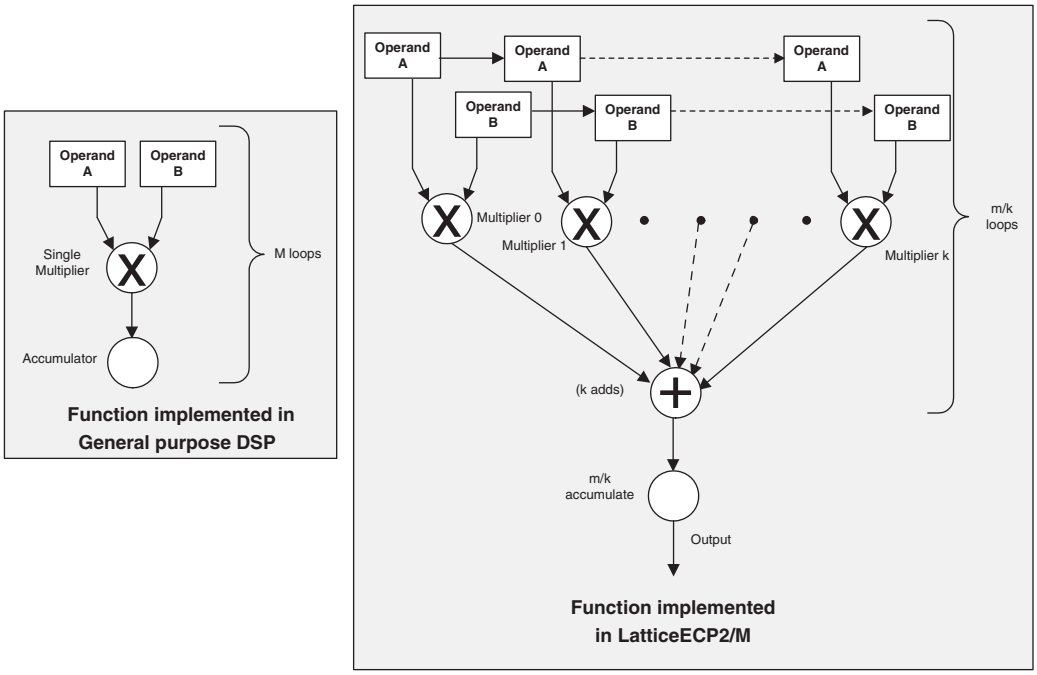
The LatticeECP2/M family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response

(FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2/M, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate level of parallelism. Figure 2-22 compares the fully serial and the mixed parallel and serial implementations.

Figure 2-22. Comparison of General DSP and LatticeECP2/M Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP2/M family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2/M family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In LatticeECP2/M family of devices the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-7 shows the capabilities of the block.

Table 2-7. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	4	2	—
MULTADDSUBSUM	2	1	—

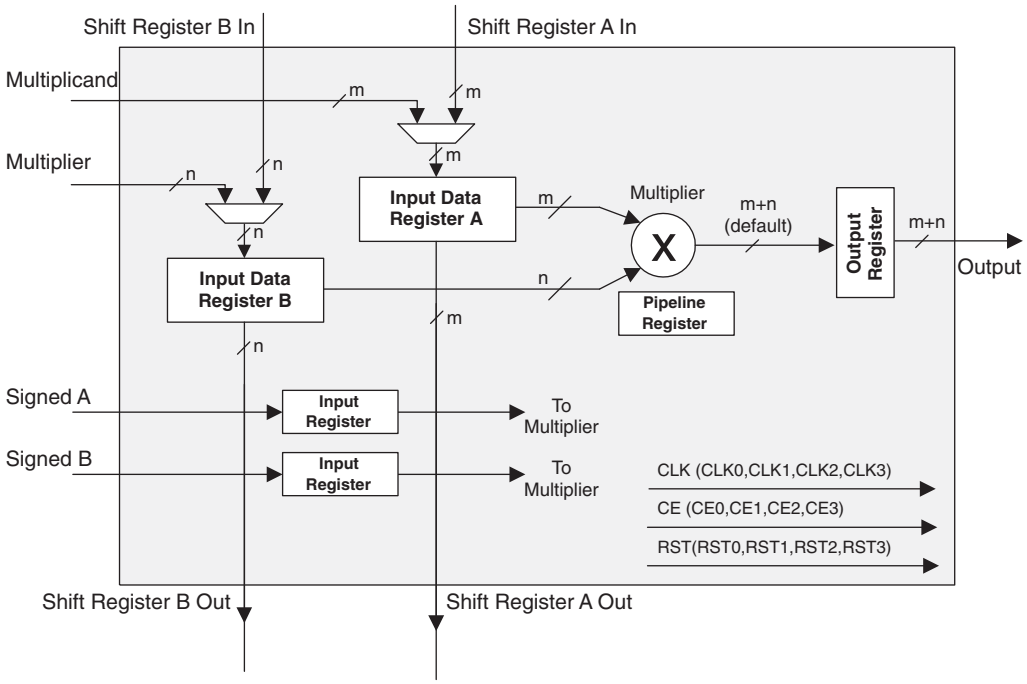
Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting 'dynamic operation' the following operations are possible:

- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-23 shows the MULT sysDSP element.

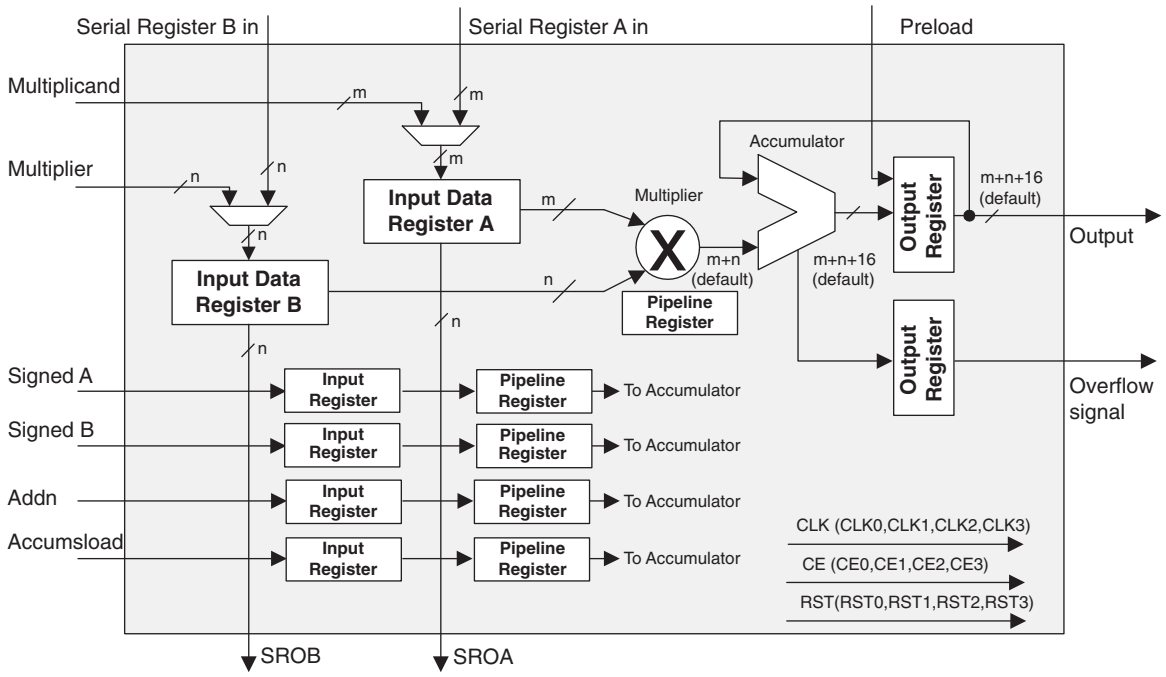
Figure 2-23. MULT sysDSP Element



MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeECP2/M family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-24 shows the MAC sysDSP element.

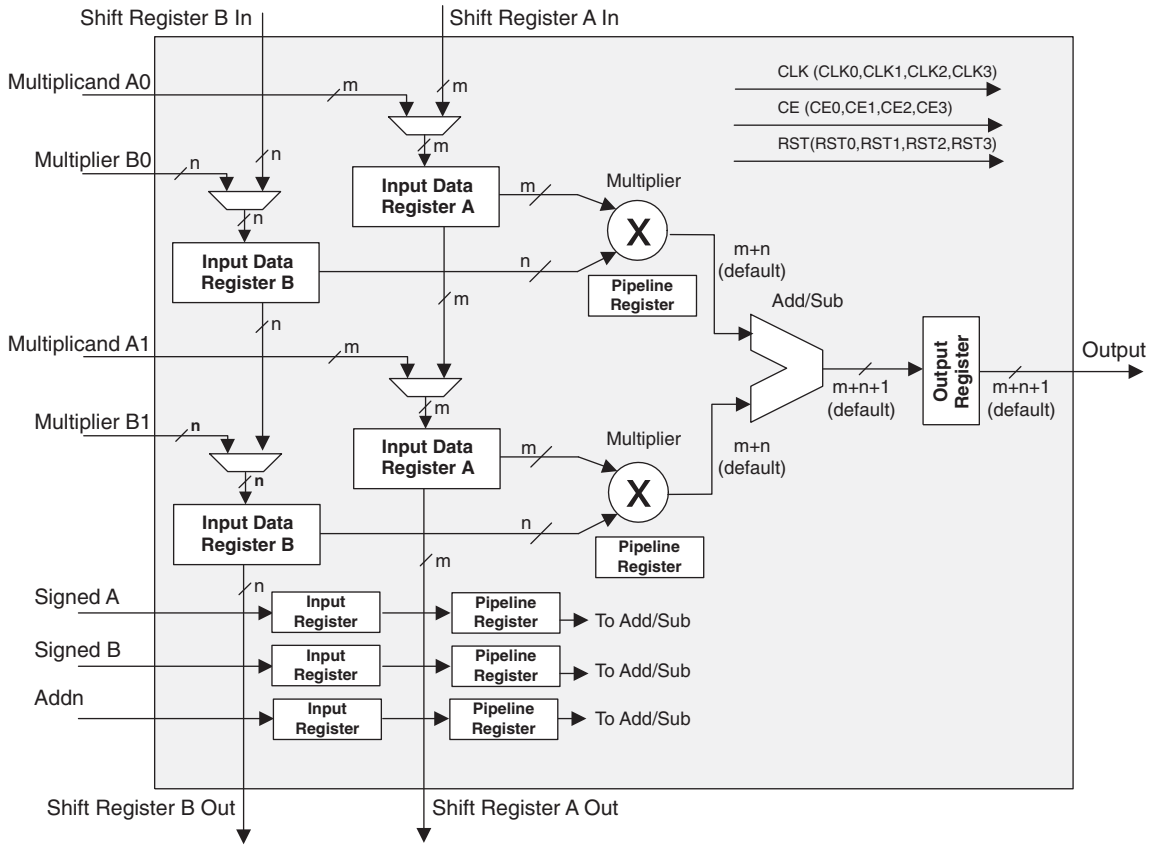
Figure 2-24. MAC sysDSP



MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

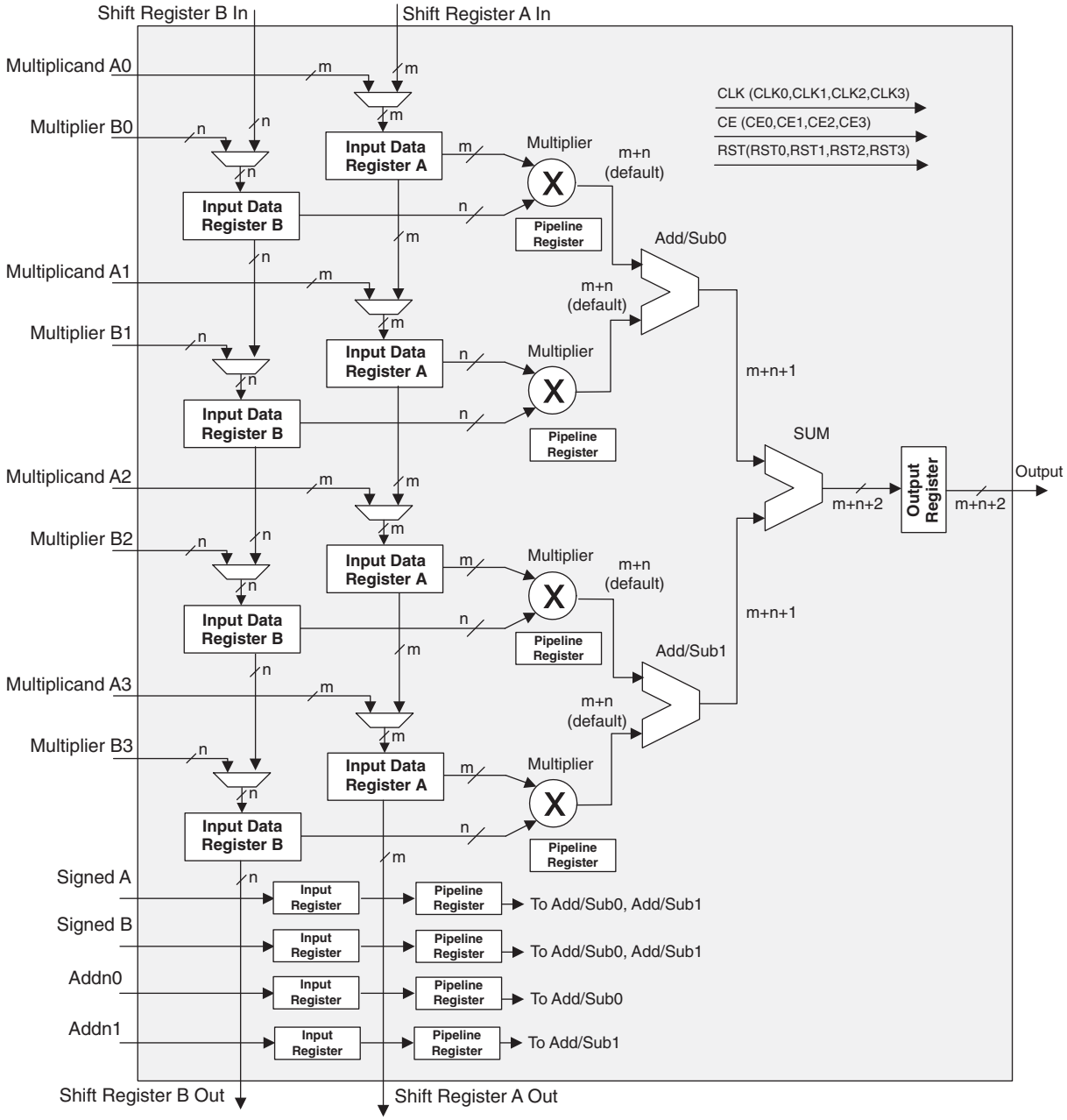
Figure 2-25. MULTADDSUB



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

Figure 2-26. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and

Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

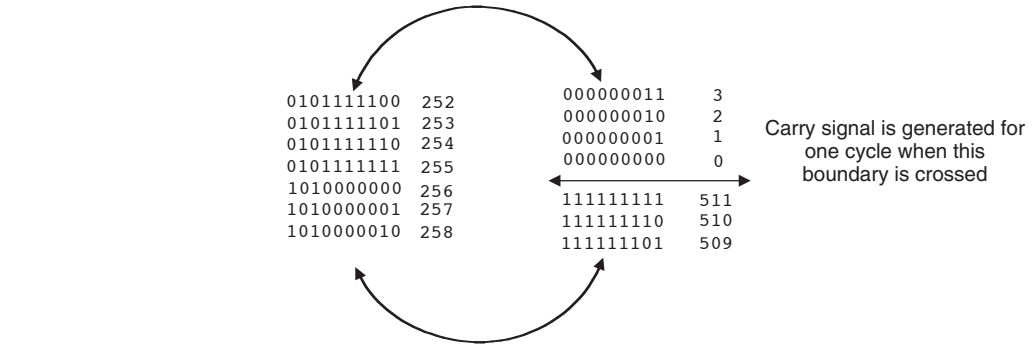
Table 2-8. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	000000000000000101	0101	000000101	000000000000000101
-6	N/A	N/A	N/A	1010	111111010	111111111111111010

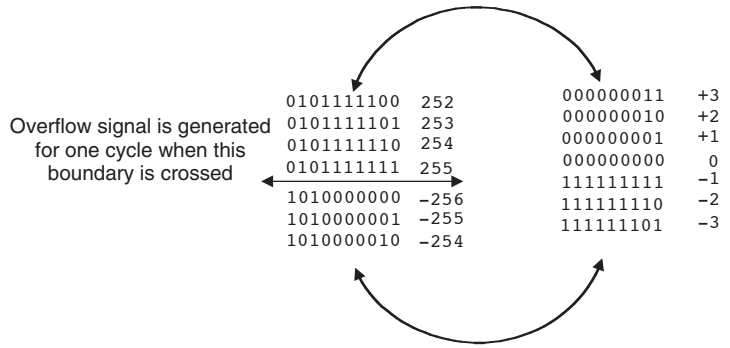
OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, "roll-over" is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signal for signed and unsigned operands are listed in Figure 2-27.

Figure 2-27. Accumulator Overflow/Underflow



Unsigned Operation



Signed Operation

IPexpress™

The user can access the sysDSP block via the ispLEVER IPexpress tool which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with ispLEVER to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

LatticeECP2/M DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2/M family.

Table 2-11. DSP Performance

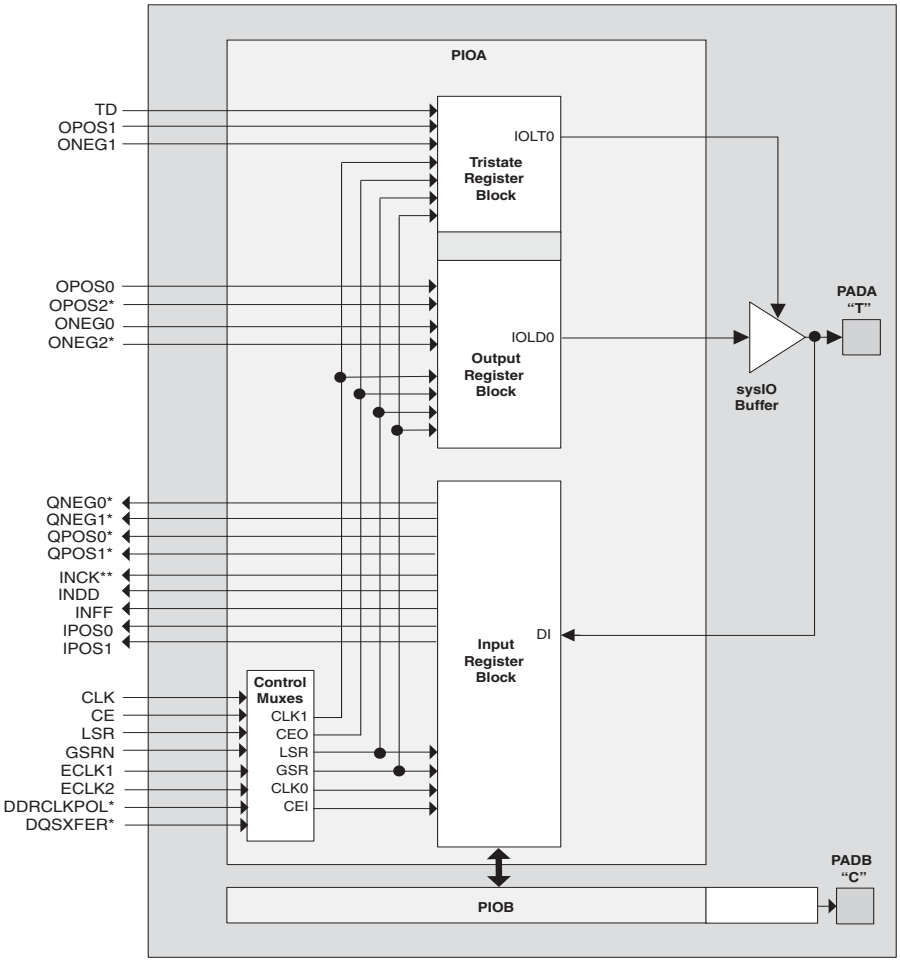
Device	DSP Block	DSP Performance GMAC
ECP2-6	3	3.9
ECP2-12	6	7.8
ECP2-20	7	9.1
ECP2-35	8	10.4
ECP2-50	18	23.4
ECP2-70	22	28.6
ECP2M20	6	7.8
ECP2M35	8	10.4
ECP2M50	22	28.6
ECP2M70	24	31.2
ECP2M100	42	54.6

For further information on the sysDSP block, please see details of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-28. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-14 provides the PIO signal list.

Figure 2-28. PIC Diagram



*Signals are available on left/right/bottom edges only.
** Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-28. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block flip-flops
CLK0, CLK1	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK[2]	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0[1], QPOS1[1]	Input to the core	Gearbox pipelined inputs to the core
QNEG0[1], QNEG1[1]	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.
2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs in left, right and bottom edges contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-29 shows the diagram of the input register block for left, right and bottom edges. The input register block for the top edge contains one memory element to register the input signal as shown in Figure 2-30. The following description applies to the input register block for PIOs in left, right and bottom edges of the device.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In DDR Mode, two registers are used to sample the data on the positive and negative edges of the DQS signal, creating two data streams, D0 and D1. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information on this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-29. Input Register Block for Left, Right and Bottom Edges

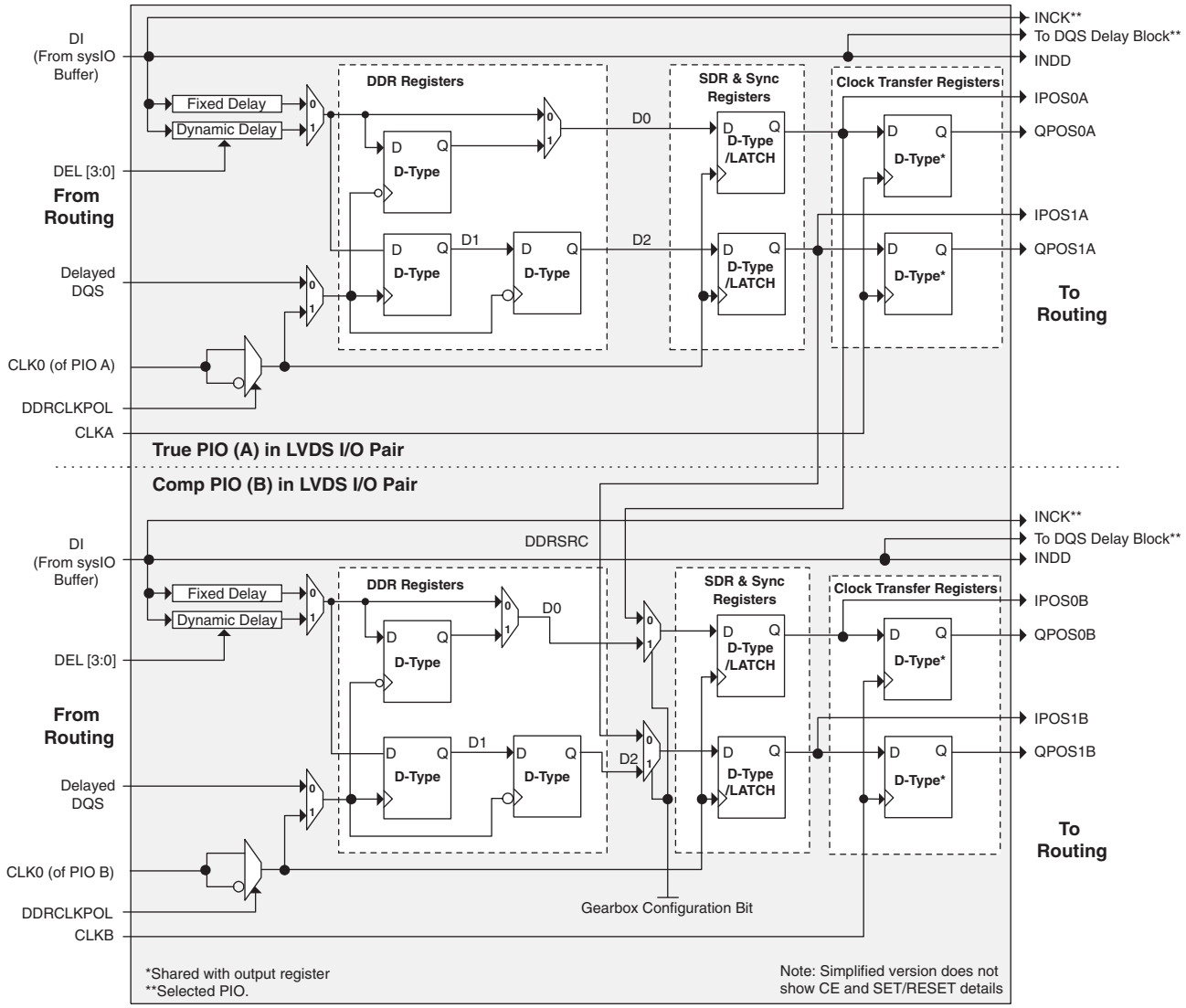
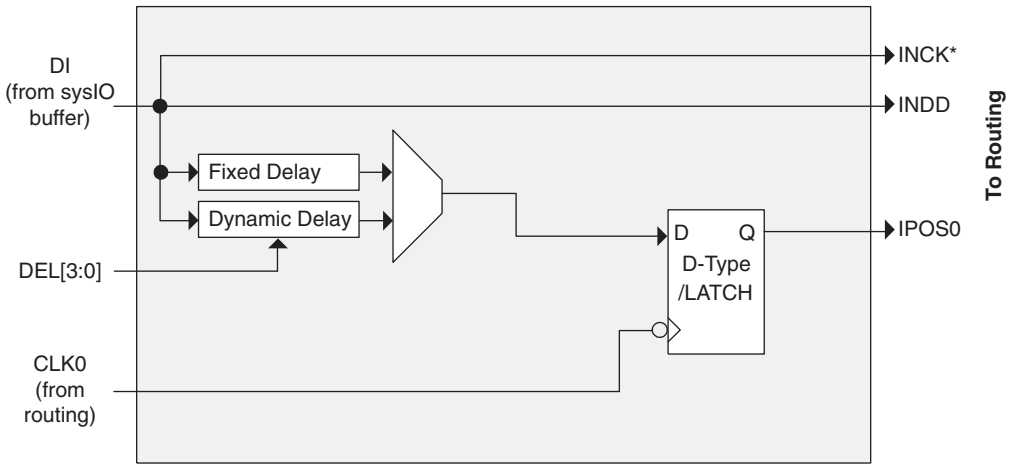


Figure 2-30. Input Register Block Top Edge



Note: Simplified version does not show CE and SET/RESET details.
*On selected blocks.

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-31 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-32 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers is fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-32 shows the diagram using this gearbox function. For more information on this topic, please see information regarding additional documentation at the end of this data sheet.

Figure 2-31. Output and Tristate Block for Left, Right and Bottom Edges

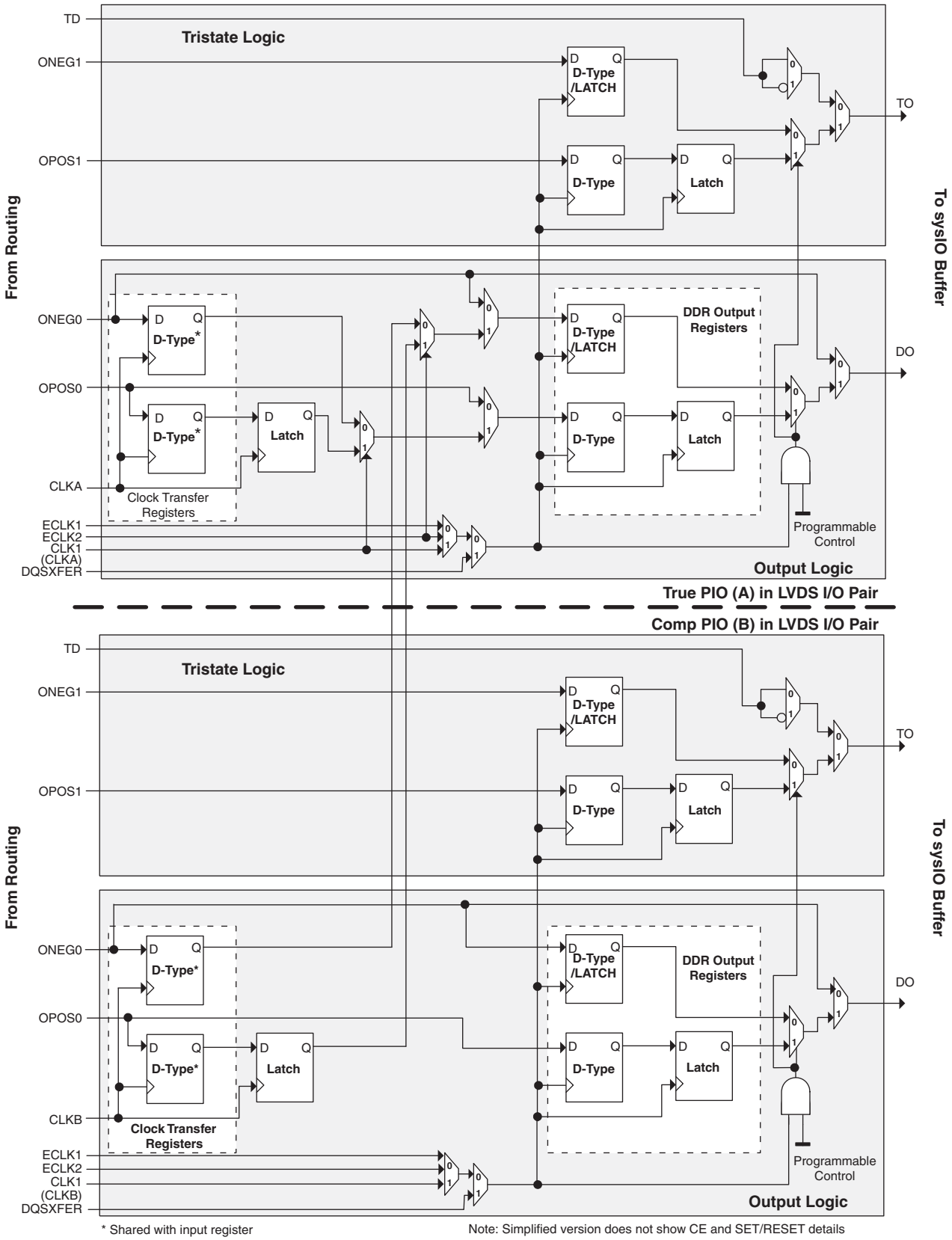
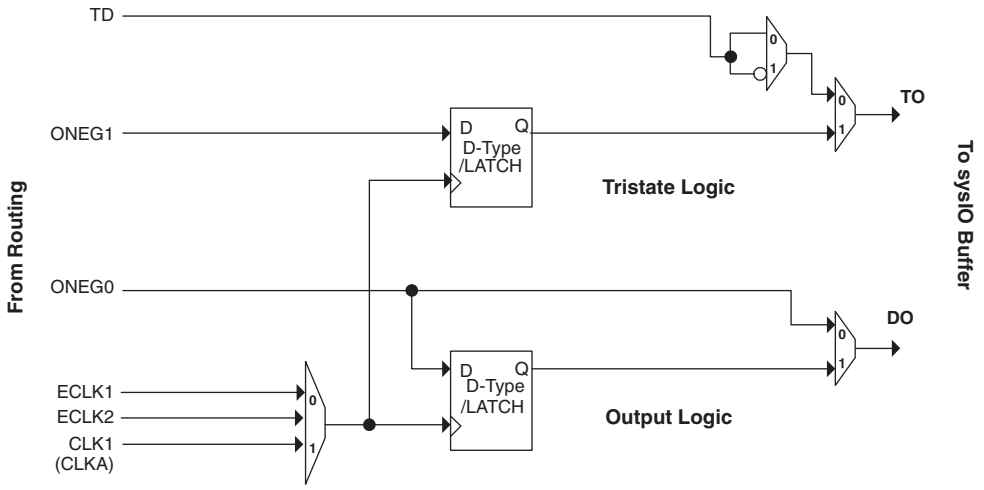


Figure 2-32. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by edge of the device as detailed below.

Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

Bottom Edge

PICs on these edges have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device

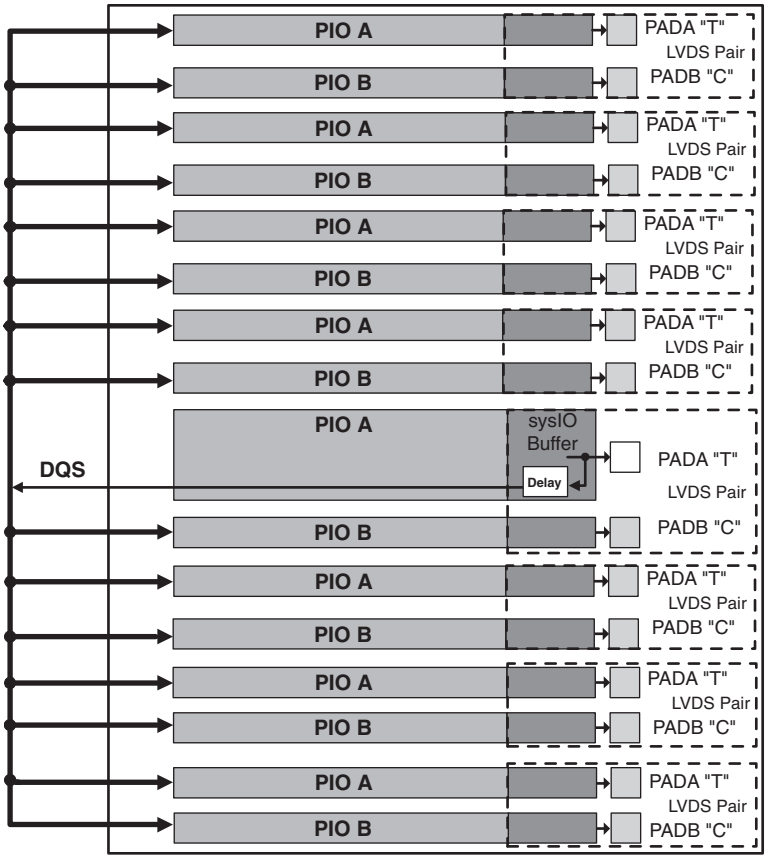
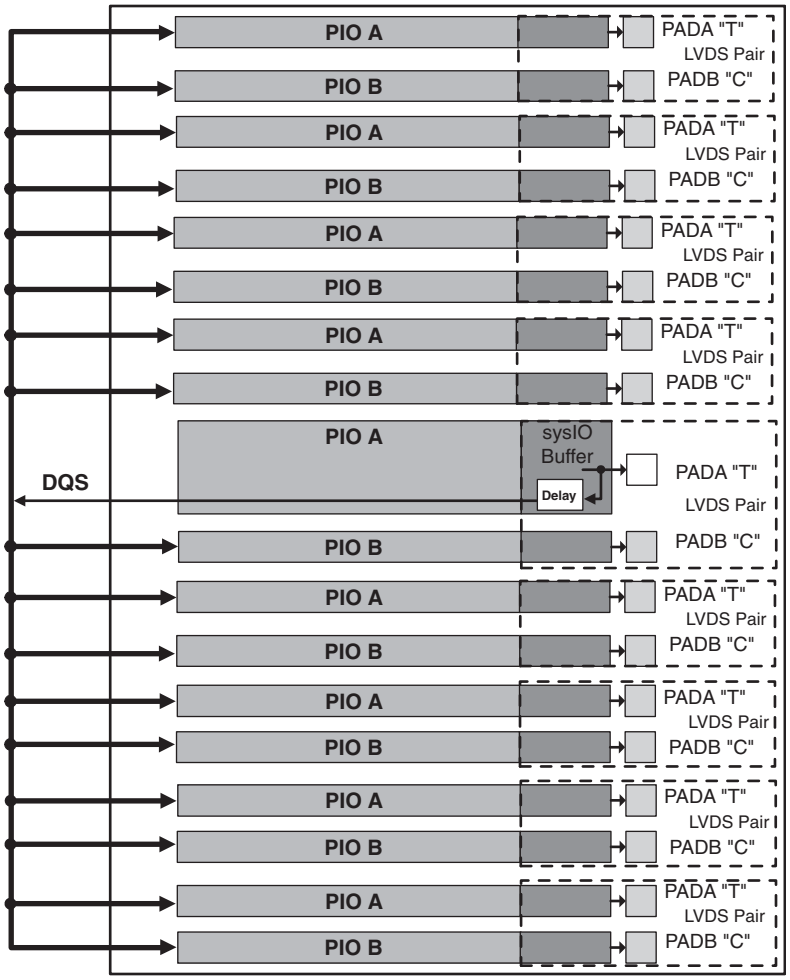


Figure 2-34. DQS Input Routing for the Bottom Edge of the Device



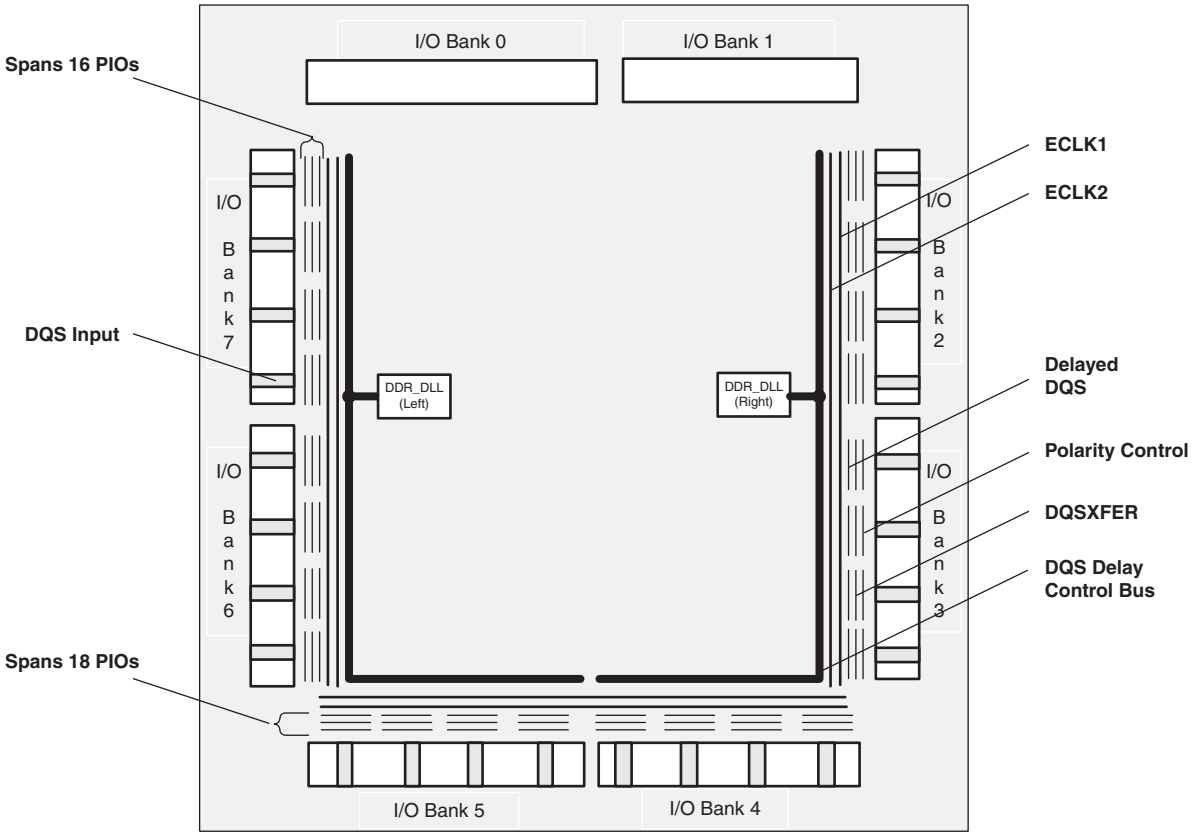
DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-35 and Figure 2-36 show how the DQS transition signals are routed to the PIOs.

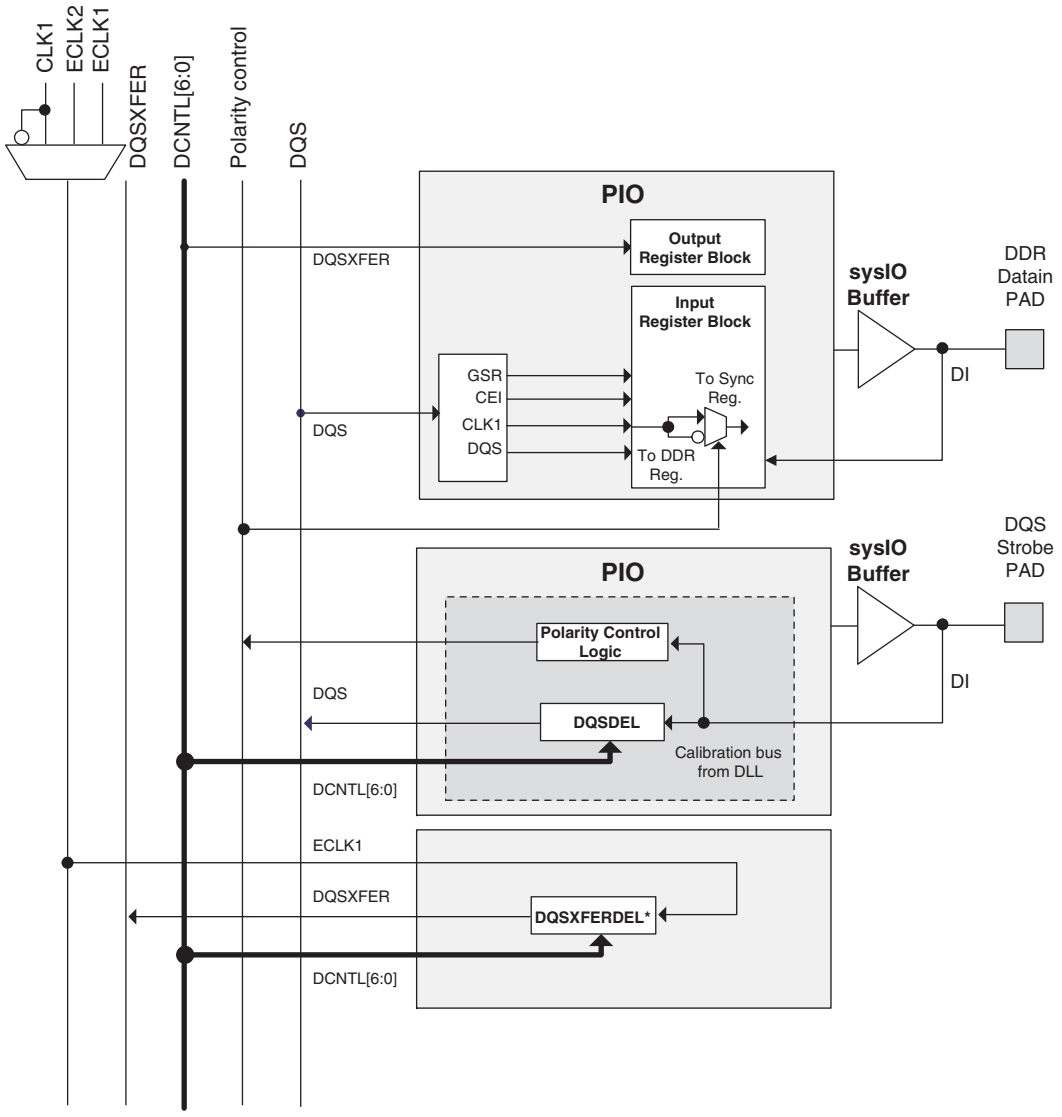
The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-35. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

Figure 2-36. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

LatticeECP2/M devices have nine sysIO buffer banks: eight banks for user I/Os arranged two per side. The ninth sysIO buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2}, that allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2}, with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-37. LatticeECP2 Banks

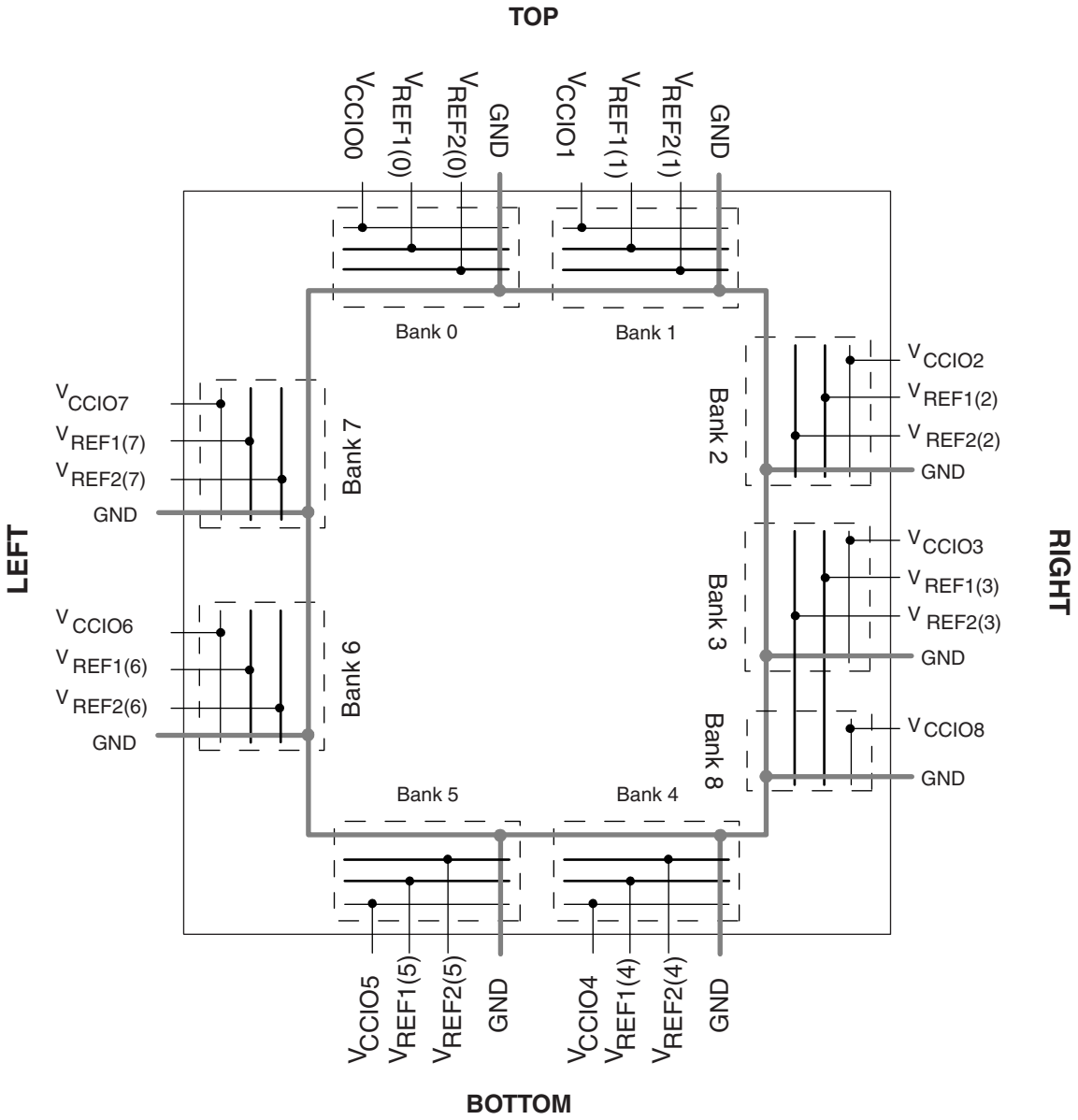
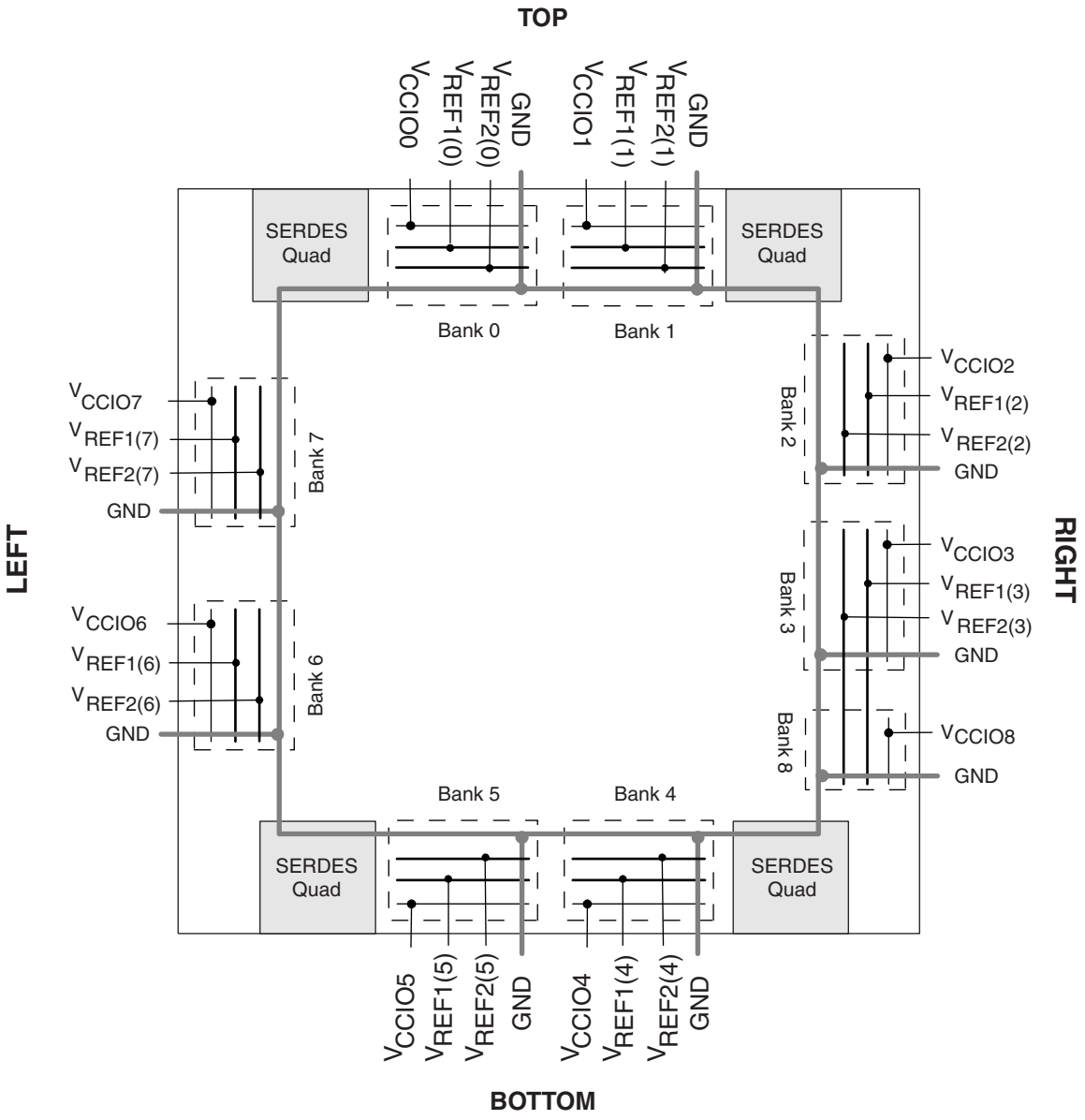


Figure 2-38. LatticeECP2M Banks



LatticeECP2/M devices contain two types of sysIO buffer pairs.

1. **Top (Bank 0 and Bank 1) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Bottom (Bank 4 and Bank 5) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the bottom banks of the device consist of two single-ended output drivers and two

sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

3. **Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

4. **Bank 8 sysIO Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysIO buffers in Bank 8 consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

In LatticeECP2 devices, only the I/Os on the bottom banks have programmable PCI clamps. In LatticeECP2M devices, the I/Os on the left and bottom banks have programmable PCI clamps.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information on controlling the output logic state with valid input logic levels during power-up in LatticeECP2/M devices, see details of additional technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeECP2/M sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by LatticeECP2/M devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12	—	—
PCI 33	—	3.3
HSTL18 Class I, II	0.9	—
HSTL15 Class I	0.75	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I, II	0.9	—
Differential Interfaces		
Differential SSTL18 Class I, II	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I	—	—
Differential HSTL18 Class I, II	—	—
LVDS, MLVDS, LVPECL, BLVDS, RSDS	—	—

1 When not specified, V_{CCIO} can be set anywhere in the valid operating range (page 3-1).

Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

Hot Socketing

LatticeECP2/M devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2/M ideal for many multiple power supply and hot-swap applications.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP2M devices feature up to 16 channels of embedded SERDES arranged in quads at the corners of the devices. Figure 2-39 shows the position of the quad blocks in relation to the PFU array for LatticeECP2M70 and LatticeECP2M100 devices. Table 2-15 shows the location of Quads for all the devices.

Each quad contains, four dedicated SERDES (Ch0 to Ch3) for high-speed, full-duplex serial data transfer. Each quad also has PCS block that interfaces to the SERDES channels and contain digital logic to support an array of popular data protocols. PCS also contain logic to interface to FPGA core.

Figure 2-39. SERDES Quads (LatticeECP2M70/LatticeECP2M100)

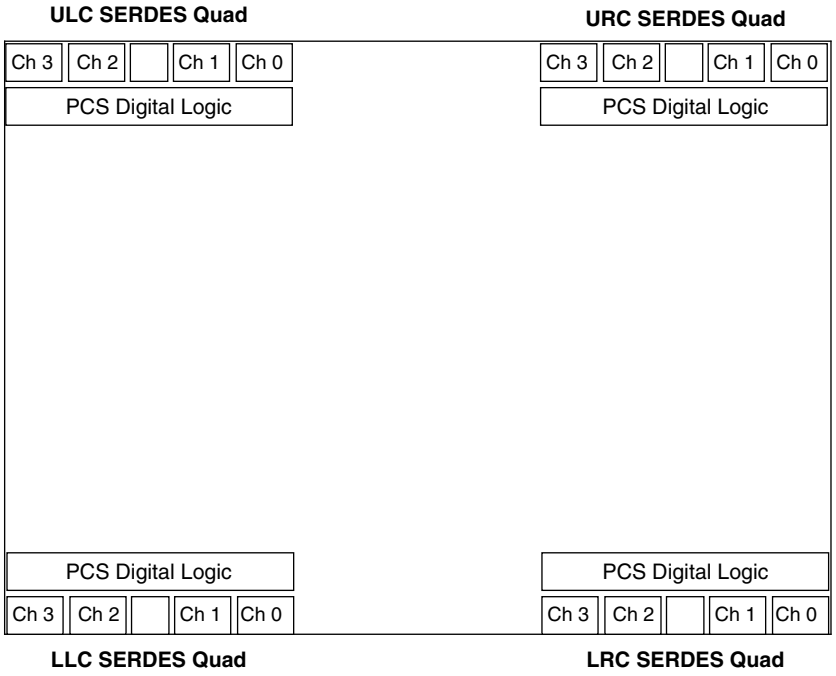


Table 2-15. Available SERDES Quads per LatticeECP2M Devices

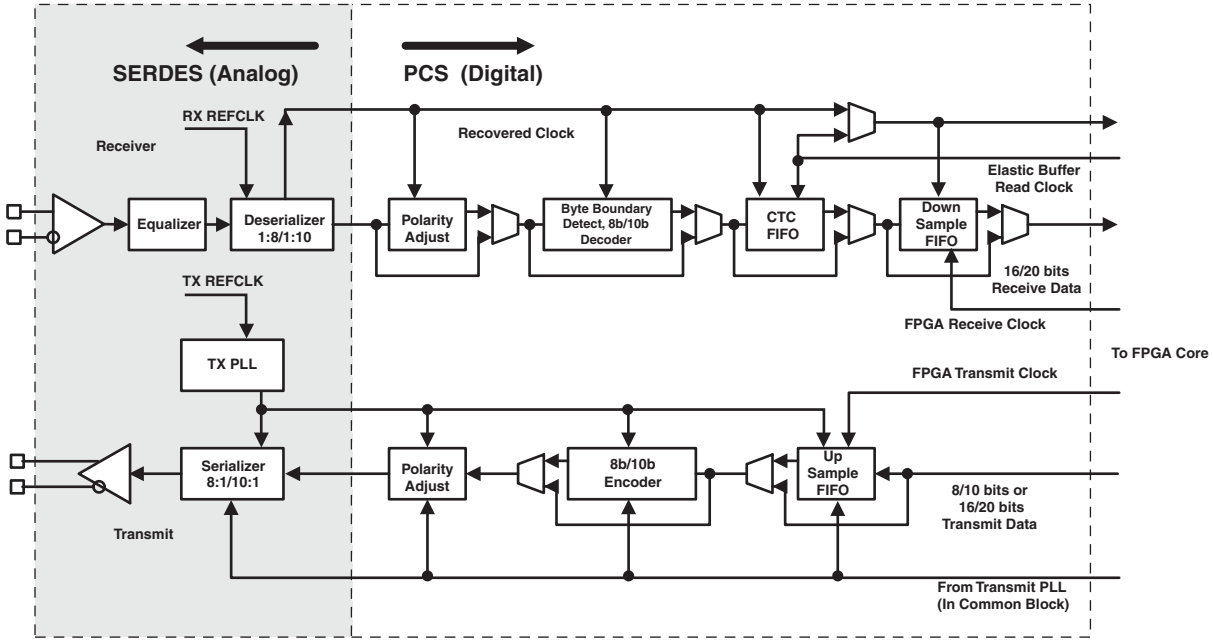
Device	URC Quad	ULC Quad	LRC Quad	LLC Quad
ECP2M20	Available	—	—	—
ECP2M35	Available	—	—	—
ECP2M50	Available	—	Available	—
ECP2M70	Available	Available	Available	Available
ECP2M100	Available	Available	Available	Available

SERDES Block

A differential receiver receives the serial encoded data stream, equalizes the signal, extracts the buried clock and de-serializes the data-stream before passing the 8- or 10-bit data to the PCS logic. The transmit channel receives the parallel (8- or 10-bit) encoded data, serializes the data and transmits the serial bit stream through the differential buffers. There is a single transmit clock per quad. Figure 2-40 shows a single channel SERDES and its interface to the PCS logic. Each SERDES receiver channel provides a recovered clock to the PCS block and to the FPGA core logic.

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel have their own independent power supplies too. In addition, there are separate power supplies for PLL, terminating resistor per quad.

Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS



PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information on SERDES, please see details of additional technical documentation at the end of this data sheet.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP2/M devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeECP2/M devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support both byte-wide and serial configuration, including the standard SPI Flash interface. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In- System Configuration specification. The sysCONFIG port is a 20-pin interface with six I/Os used as dedicated pins with the remainder used as dual-use pins. See Lattice technical note number TN1108, *LatticeECP2 sysCONFIG Usage Guide* for more information on using the dual-use pins as general purpose I/Os.

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

Enhanced Configuration Option

LatticeECP2/M devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual boot image support.

1. **Decryption Support**
   LatticeECP2/M devices provide on-chip, One Time Programmable (OTP) non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See Lattice technical note number TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP2/M can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP2/M device can revert back to the original backup configuration and try again. This all can be done without power cycling the system.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Software Error Detect (SED) Support

LatticeECP2/M devices have dedicated logic to perform CRC checks. During configuration, the configuration data bitstream can be checked with CRC logic block. In addition the LatticeECP2 device can also be programmed for

checking soft errors (SED) in SRAM. This SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to either reload from a known good boot image or generate an error signal.

For further information on Soft Error Detect (SED) support, please see details of additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP2/M devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP2/M device has an internal CMOS oscillator which is used to derive a Master Clock for configuration. The oscillator and the Master Clock run continuously and are available to user logic after configuration is completed. The software default value of the Master Clock is 2.5MHz. Table 2-16 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the Master Clock frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see details of additional technical documentation at the end of this data sheet.

Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5[1]	—	45
—	15	51
5.4	20	55
—	26	60
—	30	—
—	34	—
10.0	41	—

1. Software default frequency.

Density Shifting

The LatticeECP2/M family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. Design migration between LatticeECP2 and LatticeECP2M families is not possible.

LatticeECP2/M Family Data Sheet DC and Switching Characteristics

July 2007 Advance Data Sheet DS1006

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature (Tj) . . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1, 4, 5]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[1, 3, 4, 5]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCIO}[1, 2, 4]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply (For LatticeECP2M Family Only)				
V_{CCIB}	Input Buffer Power Supply (1.2V)	1.14	1.26	V
	Input Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2V)	1.14	1.26	V
	Output Buffer Power Supply (1.5V)	1.425	1.575	V
$V_{CCAUX33}$	Termination Resistor Switching Power Supply	3.135	3.465	V
V_{CCRX}[6]	Receive Power Supply	1.14	1.26	V
V_{CCTX}[6]	Transmit Power Supply	1.14	1.26	V
V_{CCP}[6]	PLL and Reference Clock Buffer Power	1.14	1.26	V

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}. V_{CC} and V_{CCPLL} must be connected to the same power supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCAUX} ramp rate must not exceed 30mV/µs during power-up when transitioning between 0V and 3.3V.
4. For proper power-up configuration, users must ensure that the configuration control signals such as the CFGx, INITN, PROGRAMN and DONE pins are driven to the proper logic levels when the device powers up. The device power-up is triggered by the last of V_{CC}, V_{CCAUX} or V_{CCIO8} supplies that reaches its minimum valid levels. Alternatively, if the configuration control signals are pulled up by V_{CCIO8}, the V_{CCIO8} (configuration I/O bank) voltage must be powered up prior to or at the same time as the last of VCC or VCCAUX reaches its minimum levels.
5. For power-up, V_{CC} must reach its valid minimum value before powering up V_{CCAUX} (LatticeECP2/M "S" version devices only).
6. V_{CCRX}, V_{CCTX} and V_{CCP} must be tied together in each quad and all quads need to be powered up.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O leakage current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/-1000	µA
I_{HDIN}[5]	SERDES average input current when device is powered down and inputs are driven		—	—	4	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically. V_{CC} and V_{CCPLL} must be connected to the same power supply (applies to ECP2-6, ECP2-12 and ECP2-20 only).
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed V_{CCIB} of 1.575V, 8b10b data and internal AC coupling.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
I_{IH}[1]	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	-210	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz.

LatticeECP2 Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply Current	ECP2-6	14	mA
		ECP2-12	23	mA
		ECP2-20	35	mA
		ECP2-35	44	mA
		ECP2-50	64	mA
		ECP2-70	91	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	24	mA
		ECP2-12	24	mA
		ECP2-20	24	mA
		ECP2-35	24	mA
		ECP2-50	24	mA
		ECP2-70	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2-6	1	mA
		ECP2-12	2	mA
		ECP2-20	3	mA
		ECP2-35	3	mA
		ECP2-50	4	mA
		ECP2-70	5	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at normal voltage.

LatticeECP2M Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply Current	ECP2M20	39	mA
		ECP2M35	61	mA
		ECP2M50		mA
		ECP2M70		mA
		ECP2M100		mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	24	mA
		ECP2M35	24	mA
		ECP2M50		mA
		ECP2M70		mA
		ECP2M100		mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2M20	2	mA
		ECP2M35	3	mA
		ECP2M50		mA
		ECP2M70		mA
		ECP2M100		mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at normal voltage.

LatticeECP2 Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5, 6]	Units
I_{CC}	Core Power Supply Current	ECP2-6	34	mA
		ECP2-12	54	mA
		ECP2-20	82	mA
		ECP2-35	135	mA
		ECP2-50	187	mA
		ECP2-70	267	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	30	mA
		ECP2-12	30	mA
		ECP2-20	30	mA
		ECP2-35	30	mA
		ECP2-50	30	mA
		ECP2-70	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

LatticeECP2M Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5, 6]	Units
I_{CC}	Core Power Supply Current	ECP2M20	41	mA
		ECP2M35	107	mA
		ECP2M50	169	mA
		ECP2M70	254	mA
		ECP2M100	378	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	30	mA
		ECP2M35	30	mA
		ECP2M50	30	mA
		ECP2M70	30	mA
		ECP2M100	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. T_J = 25ºC, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

SERDES Power Supply Requirements (LatticeECP2M Family Only)[1]

Over Recommended Operating Conditions

Symbol	Description	Typ.[2]	Units
Standby (Power Down)			
$I_{CCTX-SB}$	V_{CCTX} current (per channel)	10	µA
$I_{CCRX-SB}$	V_{CCRX} current (per channel)	75	µA
$I_{CCIB-SB}$	Input buffer current (per channel)	0	µA
$I_{CCOB-SB}$	Output buffer current (per channel)	0	µA
I_{CCP-SB}	SERDES PLL current (per quad)	30	µA
$I_{CCAX33-SB}$	SERDES termination current (per quad)	10	µA
Operating (Data Rate = 3.125 Gbps)			
$I_{CCTX-OP}$	V_{CCTX} current (per channel)	19	mA
$I_{CCRX-OP}$	V_{CCRX} current (per channel)	34	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	13	mA
I_{CCP-OP}	SERDES PLL current (per quad)	26	mA
$I_{CCAX33-OP}$	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.
2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power[1]

Symbol	Description	Typ.[2]	Units
$P_{S-1CH-31}$	SERDES power (one channel @ 3.125 Gbps)	90	mW
$P_{S-1CH-25}$	SERDES power (one channel @ 2.5 Gbps)	87	mW
$P_{S-1CH-12}$	SERDES power (one channel @ 1.25 Gbps)	86	mW
$P_{S-1CH-02}$	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25ºC and 1.2V.

sysIO Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3[2]	3.135	3.3	3.465	—	—	—
LVCMOS 2.5[2]	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2[2]	1.14	1.2	1.26	—	—	—
LVTTL[2]	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18[2] Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2[2] Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3[2] Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL[2] 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL[2] 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeECP2/M devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

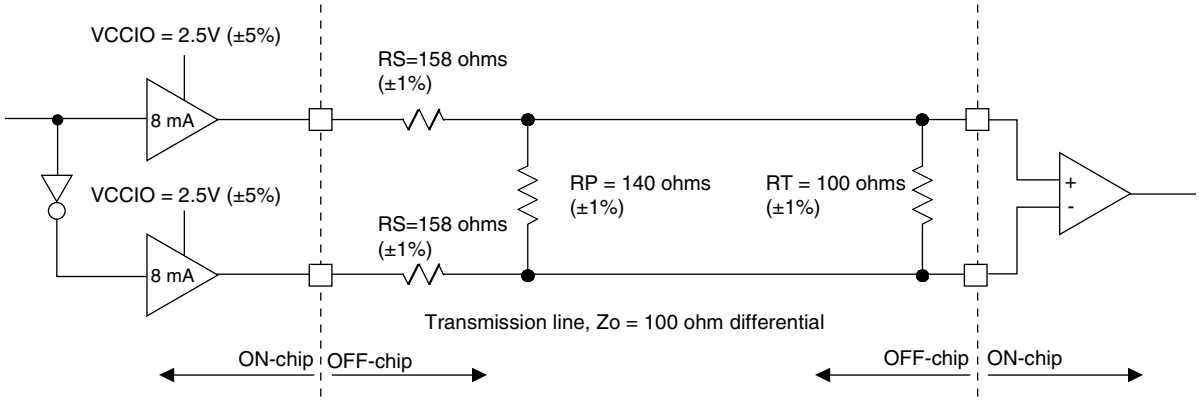


Table 3-2. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	158	Ω
R_P	Driver Parallel Resistor (+/-1%)	140	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

BLVDS

The LatticeECP2/M devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

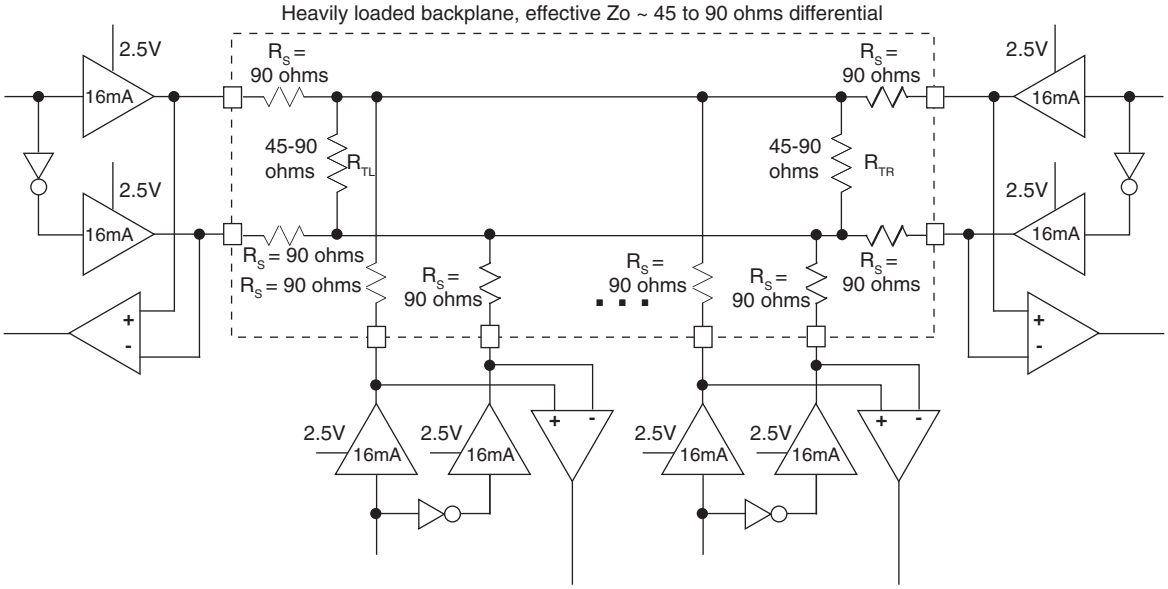


Table 3-3. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V_{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

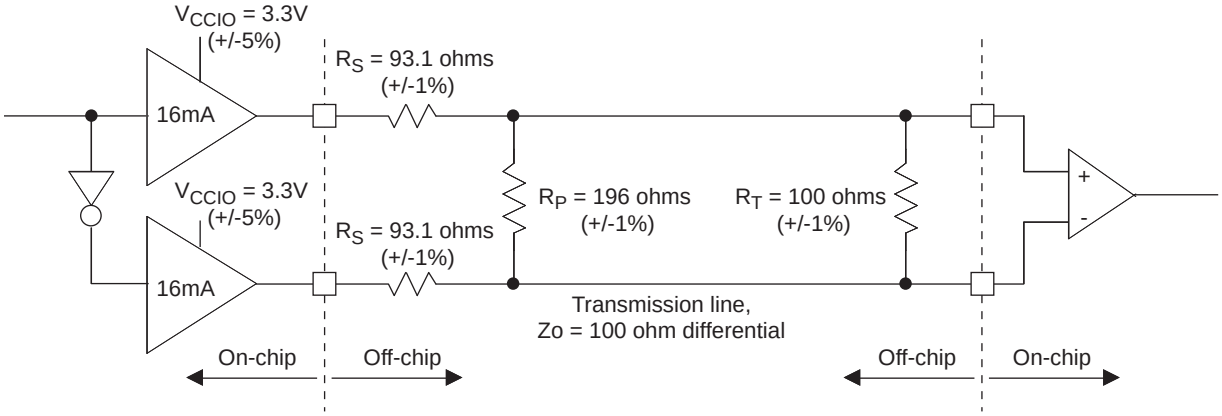


Table 3-4. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

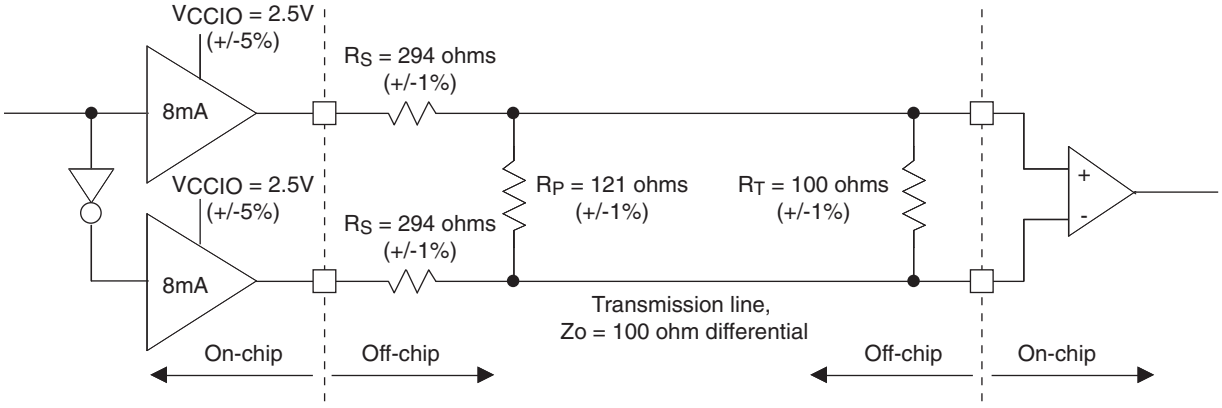


Table 3-5. RSDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

MLVDS

The LatticeECP2/M devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Multipoint Low Voltage Differential Signaling)

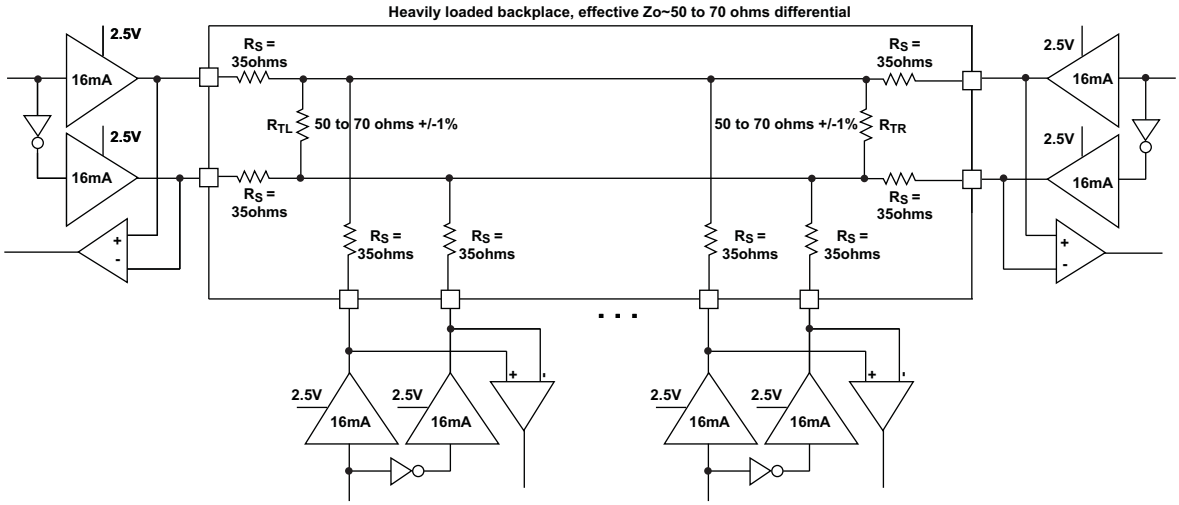


Table 3-6. MLVDS DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	3.8	ns
32-bit Decoder	4.5	ns
64-bit Decoder	5.0	ns
4:1 MUX	3.2	ns
8:1 MUX	3.4	ns
16:1 MUX	3.5	ns
32:1 MUX	4.0	ns

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.A 0.10

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	599	MHz
32-bit Decoder	542	MHz
64-bit Decoder	417	MHz
4:1 MUX	847	MHz
8:1 MUX	803	MHz
16:1 MUX	660	MHz
32:1 MUX	577	MHz
8-bit Adder	591	MHz
16-bit Adder	500	MHz
64-bit Adder	306	MHz
16-bit Counter	488	MHz
32-bit Counter	378	MHz
64-bit Counter	260	MHz
64-bit Accumulator	253	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	370	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)	294	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	280	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	819	MHz
32x4 Pseudo-Dual Port RAM	521	MHz
64x8 Pseudo-Dual Port RAM	435	MHz

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
DSP Functions		
18x18 Multiplier (All Registers)	420	MHz
9x9 Multiplier (All Registers)	420	MHz
36x36 Multiplier (All Registers)	372	MHz
18x18 Multiplier/Accumulate (Input and Output Registers)	323	MHz
18x18 Multiplier-Add/Sub-Sum (All Registers)	420	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	304	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	227	MHz
8x8 Matrix Multiplier	223	MHz

Timing v.A 0.10

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The ispLEVER design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeECP2/M External Switching Characteristics[9]

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_IO}	Clock Frequency of I/O Register and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)[1]									
t_{COE}	Clock to Output - PIO Output Register	LFE2-6	—	2.60	—	2.90	—	3.20	ns
		LFE2-12	—	2.60	—	2.90	—	3.20	ns
		LFE2-20	—	2.60	—	2.90	—	3.20	ns
		LFE2-35	—	2.60	—	2.90	—	3.20	ns
		LFE2-50	—	2.60	—	2.90	—	3.20	ns
		LFE2-70	—	2.60	—	2.90	—	3.20	ns
		LFE2M20	—	2.60	—	2.90	—	3.20	ns
		LFE2M35	—	2.60	—	2.90	—	3.20	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	LFE2-6	0.90	—	1.10	—	1.30	—	ns
		LFE2-12	0.90	—	1.10	—	1.30	—	ns
		LFE2-20	0.90	—	1.10	—	1.30	—	ns
		LFE2-35	0.90	—	1.10	—	1.30	—	ns
		LFE2-50	0.90	—	1.10	—	1.30	—	ns
		LFE2-70	0.90	—	1.10	—	1.30	—	ns
		LFE2M20	0.90	—	1.10	—	1.30	—	ns
		LFE2M35	0.90	—	1.10	—	1.30	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.00	—	1.30	—	1.60	—	ns
		LFE2-12	1.00	—	1.30	—	1.60	—	ns
		LFE2-20	1.00	—	1.30	—	1.60	—	ns
		LFE2-35	1.00	—	1.30	—	1.60	—	ns
		LFE2-50	1.00	—	1.30	—	1.60	—	ns
		LFE2-70	1.00	—	1.30	—	1.60	—	ns
		LFE2M20	1.20	—	1.60	—	1.90	—	ns
		LFE2M35	1.20	—	1.60	—	1.90	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]									
t_{COPLL}[10]	Clock to Output - PIO Output Register	LFE2-6	—	2.30	—	2.60	—	2.80	ns
		LFE2-12	—	2.30	—	2.60	—	2.80	ns
		LFE2-20	—	2.30	—	2.60	—	2.80	ns
		LFE2-35	—	2.30	—	2.60	—	2.80	ns
		LFE2-50	—	2.30	—	2.60	—	2.80	ns
		LFE2-70	—	2.30	—	2.60	—	2.80	ns
		LFE2M20	—	2.30	—	2.60	—	2.80	ns
		LFE2M35	—	2.30	—	2.60	—	2.80	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LFE2-6	0.70	—	0.80	—	0.90	—	ns
		LFE2-12	0.70	—	0.80	—	0.90	—	ns
		LFE2-20	0.70	—	0.80	—	0.90	—	ns
		LFE2-35	0.70	—	0.80	—	0.90	—	ns
		LFE2-50	0.70	—	0.80	—	0.90	—	ns
		LFE2-70	0.70	—	0.80	—	0.90	—	ns
		LFE2M20	0.70	—	0.80	—	0.90	—	ns
		LFE2M35	0.70	—	0.80	—	0.90	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LFE2-6	1.00	—	1.20	—	1.40	—	ns
		LFE2-12	1.00	—	1.20	—	1.40	—	ns
		LFE2-20	1.00	—	1.20	—	1.40	—	ns
		LFE2-35	1.00	—	1.20	—	1.40	—	ns
		LFE2-50	1.00	—	1.20	—	1.40	—	ns
		LFE2-70	1.00	—	1.20	—	1.40	—	ns
		LFE2M20	1.00	—	1.20	—	1.40	—	ns
		LFE2M35	1.00	—	1.20	—	1.40	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.80	—	2.00	—	2.20	—	ns
		LFE2-12	1.80	—	2.00	—	2.20	—	ns
		LFE2-20	1.80	—	2.00	—	2.20	—	ns
		LFE2-35	1.80	—	2.00	—	2.20	—	ns
		LFE2-50	1.80	—	2.00	—	2.20	—	ns
		LFE2-70	1.80	—	2.00	—	2.20	—	ns
		LFE2M20	1.80	—	2.00	—	2.20	—	ns
		LFE2M35	1.80	—	2.00	—	2.20	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR}	DDR Clock Frequency[6]	ECP2/M	95	200	95	166	95	133	MHz
DDR2 I/O Pin Parameters[3]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR2}	DDR Clock Frequency	ECP2/M	133	266	133	200	133	166	MHz
SPI4.2 I/O Pin Parameters Static Alignment[4, 8, 11]									
	Maximum Data Rate	ECP2-20	—	750	—	622	—	622	Mbps
		ECP2-35	—	750	—	622	—	622	Mbps
		ECP2-50	—	750	—	622	—	622	Mbps
		ECP2-70	—	750	—	622	—	622	Mbps
		ECP2M20	—	650	—	622	—	622	Mbps
		ECP2M35	—	650	—	622	—	622	Mbps
$t_{DVACLKSPI}$	Data Valid After CLK (Receive)	ECP2-20	—	0.26	—	0.26	—	0.26	UI
		ECP2-35	—	0.26	—	0.26	—	0.26	UI
		ECP2-50	—	0.26	—	0.26	—	0.26	UI
		ECP2-70	—	0.26	—	0.26	—	0.26	UI
		ECP2M20	—	0.26	—	0.26	—	0.26	UI
		ECP2M35	—	0.26	—	0.26	—	0.26	UI

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DVECLKSPI}$	Data Hold After CLK (Receive)	ECP2-20	0.74	—	0.74	—	0.74	—	UI
		ECP2-35	0.74	—	0.74	—	0.74	—	UI
		ECP2-50	0.74	—	0.74	—	0.74	—	UI
		ECP2-70	0.74	—	0.74	—	0.74	—	UI
		ECP2M20	0.78	—	0.78	—	0.78	—	UI
		ECP2M35	0.78	—	0.78	—	0.78	—	UI
t_{DIASPI}	Data Invalid After Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	280	—	280	—	280	ps
		ECP2M35	—	280	—	280	—	280	ps
t_{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	280	—	280	—	280	ps
		ECP2M35	—	280	—	280	—	280	ps
XGMII I/O Pin Parameters (312 Mbps)[5]									
$t_{SUXGMII}$	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t_{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
$t_{DVBCKXGMII}$	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
$t_{DVACKXGMII}$	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f_{MAX_EDGE}[7]	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to technical note TN1159, LatticeECP2M Pin Assignment Recommendations for best performance.

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Figure 3-6. SPI4.2 Parameters

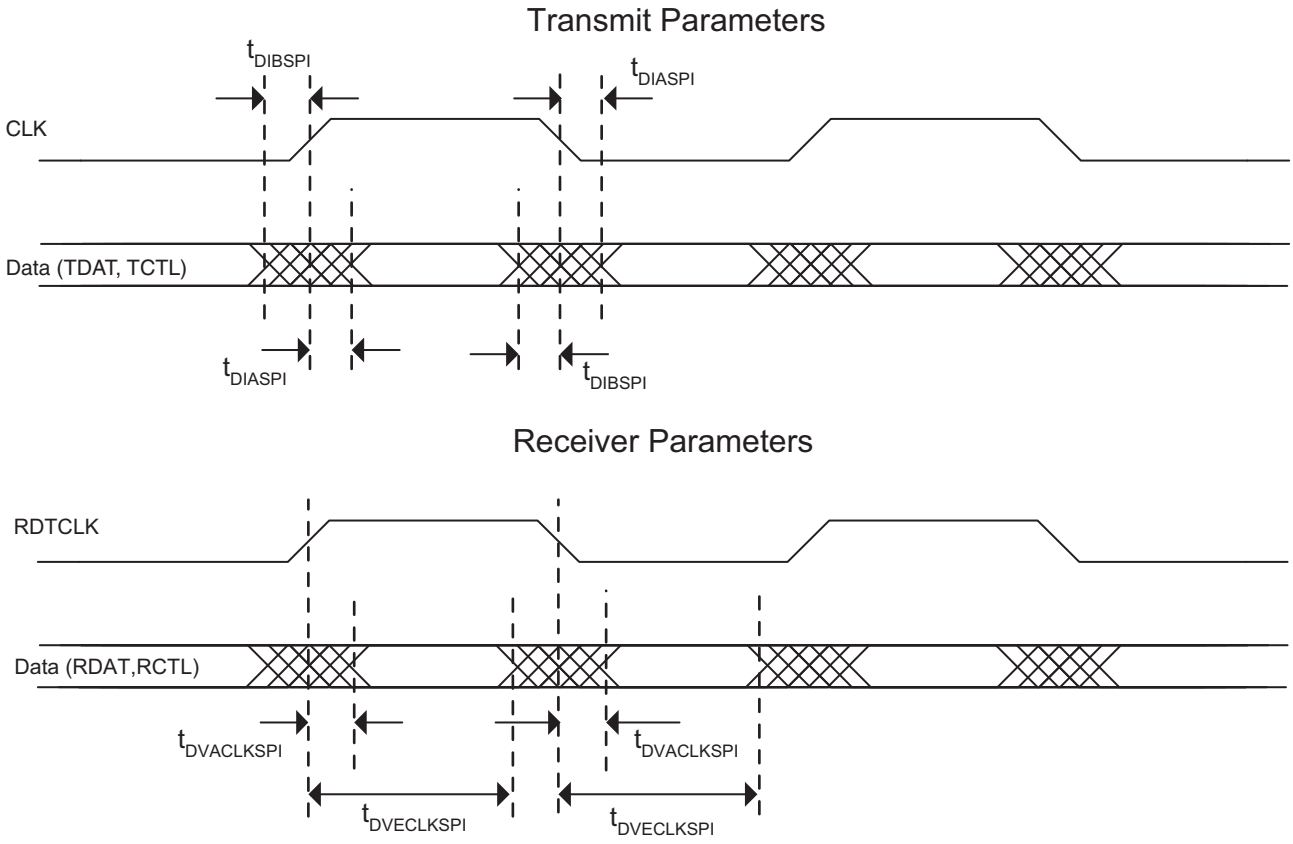


Figure 3-7. DDR and DDR2 Parameters

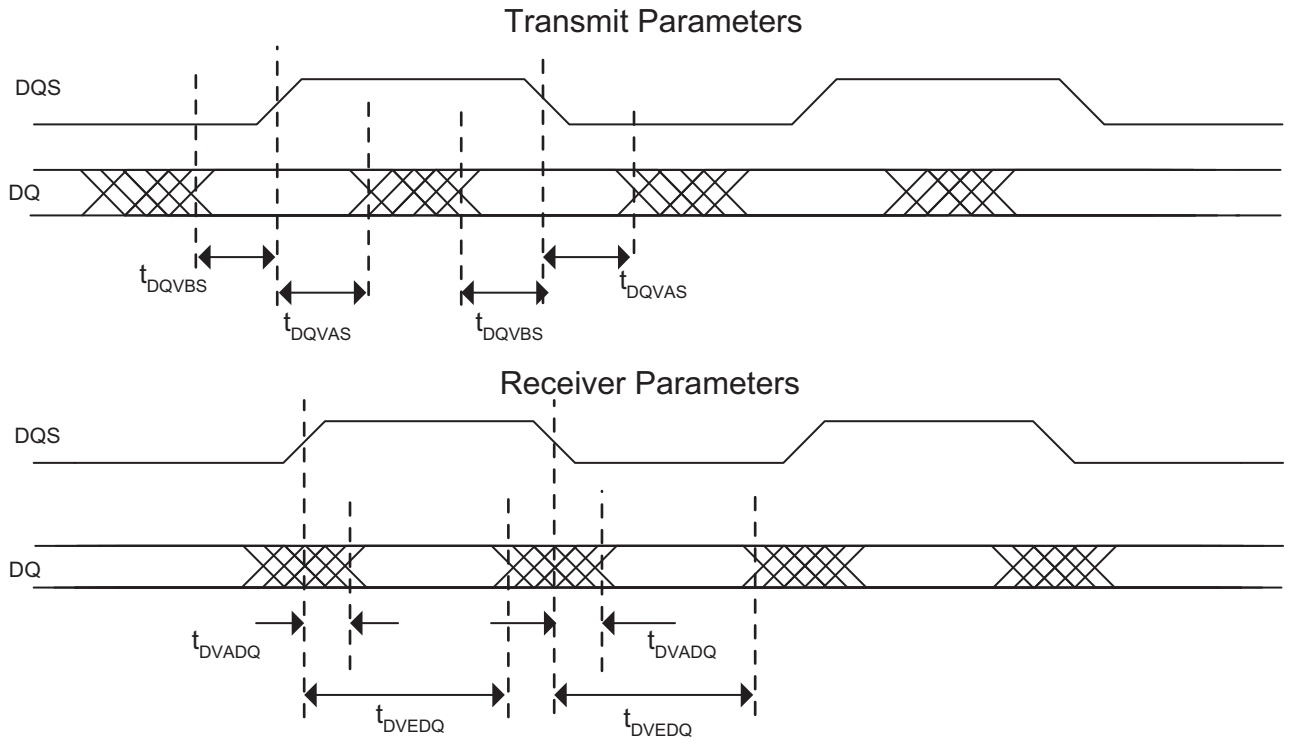
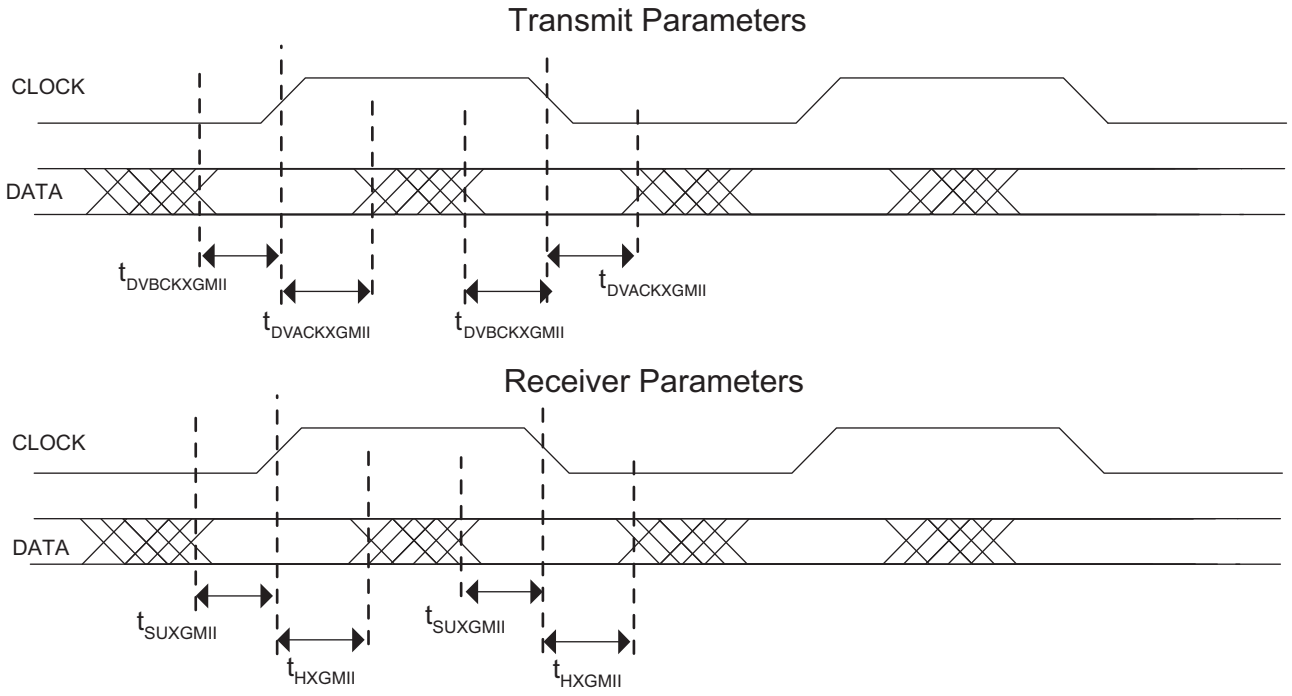


Figure 3-8. XGMII Parameters



LatticeECP2/M Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.180	—	0.198	—	0.216	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.331	—	0.358	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.600	—	0.655	—	0.711	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.128	—	0.129	—	0.129	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.051	—	-0.049	—	-0.046	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.071	—	0.081	—	ns
t_{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.285	—	0.309	—	0.333	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.902	—	1.083	—	1.263	ns
t_{SUDATA_PFU}	Data Setup Time	-0.172	—	-0.205	—	-0.238	—	ns
t_{HDATA_PFU}	Data Hold Time	0.199	—	0.235	—	0.271	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.245	—	-0.284	—	-0.323	—	ns
t_{HADDR_PFU}	Address Hold Time	0.246	—	0.285	—	0.324	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.122	—	-0.145	—	-0.168	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.132	—	0.156	—	0.180	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.613	—	0.681	—	0.749	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.115	—	1.343	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.51	—	2.75	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.33	—	0.36	—	0.39	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.157	—	-0.181	—	-0.205	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.173	—	0.195	—	0.217	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.115	—	-0.130	—	-0.145	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.138	—	0.155	—	0.172	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.128	—	-0.149	—	-0.170	—	ns

LatticeECP2/M Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	—	1.00	—	1.00	—	1.00	ns
SPLL Parameters								
t_{RSTREC_SPLL}	Reset Recovery to Rising Clock	—	1.00	—	1.00	—	1.00	ns
DSP Block Timing[2,3]								
t_{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t_{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t_{tHP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t_{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
$t_{SUADDSUB}$	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
$t_{HADDSUB}$	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

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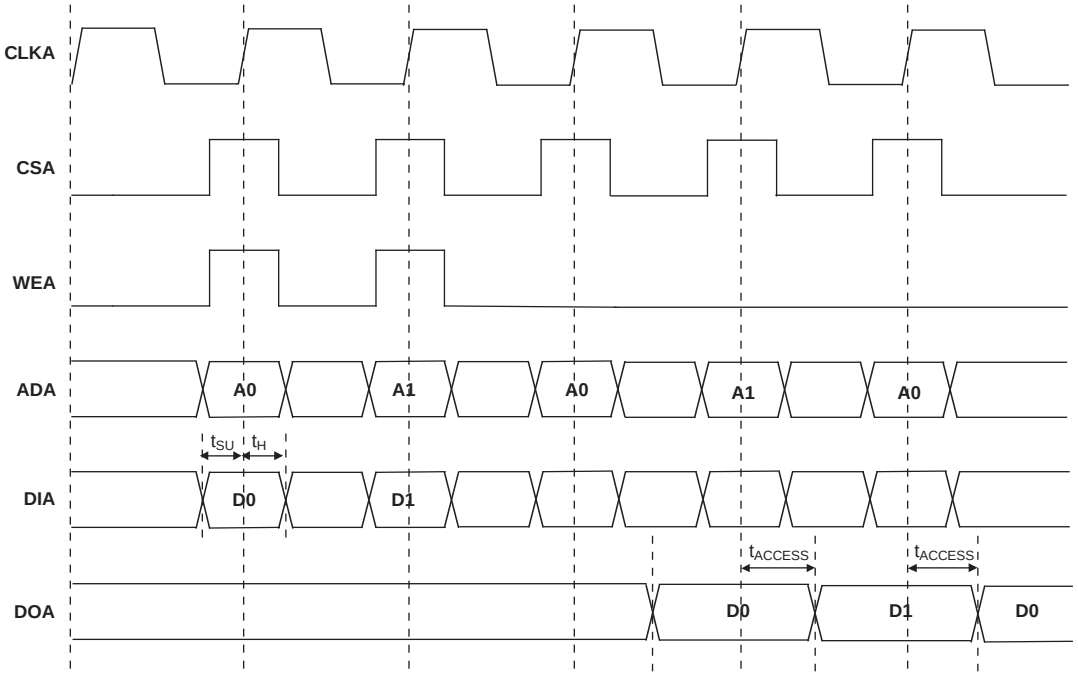
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

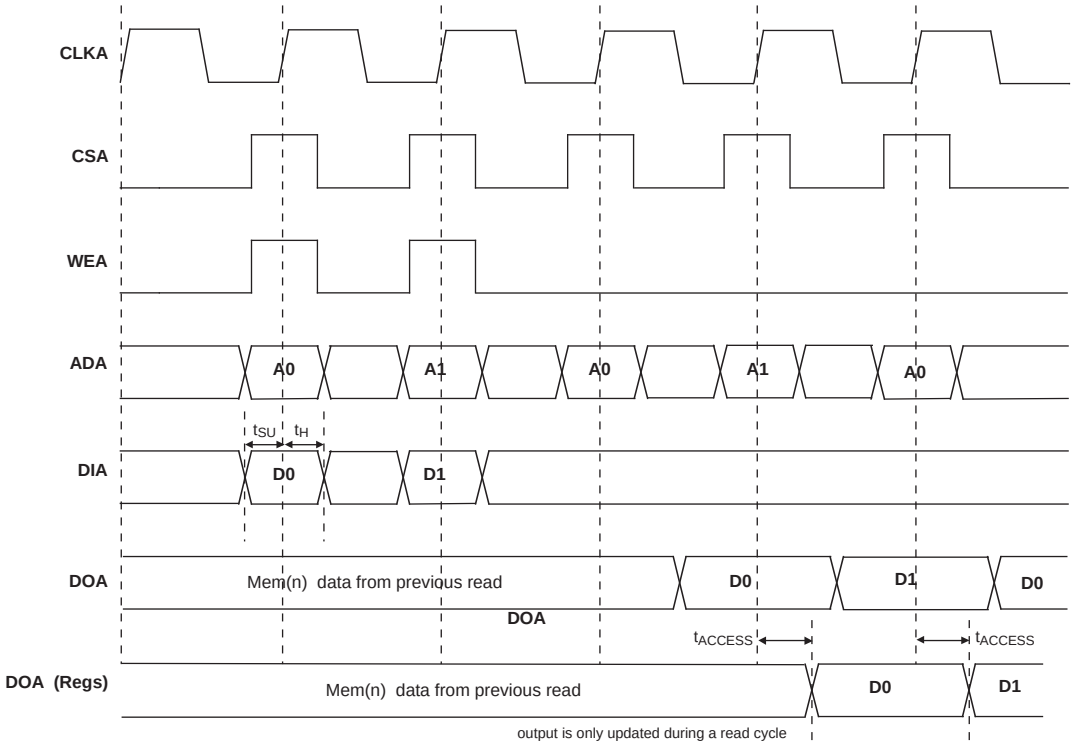
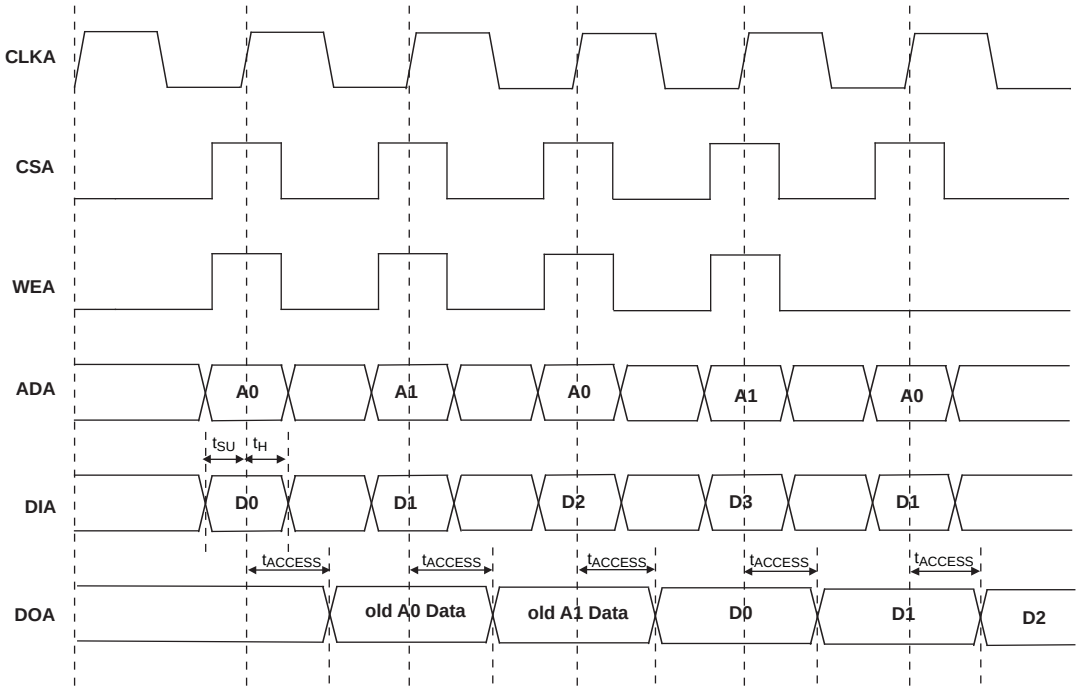
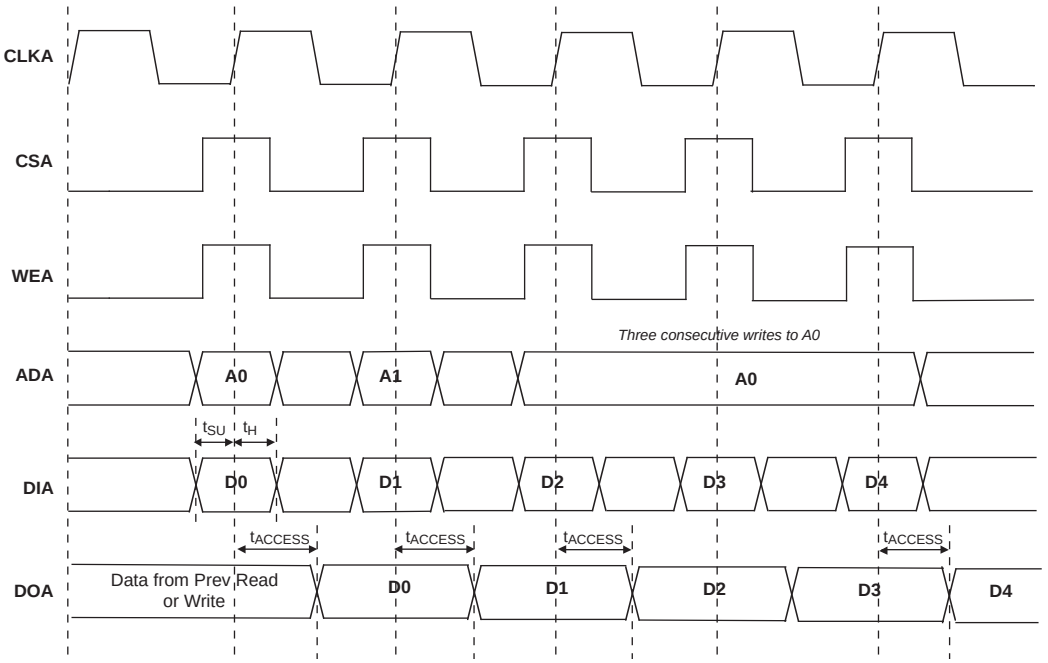


Figure 3-11. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-12. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP2/M Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25E	LVDSE	-0.04	-0.07	-0.10	ns
LVDS25	LVDS	-0.04	-0.02	0.00	ns
BLVDS25	BLVDS	-0.04	-0.09	-0.15	ns
MLVDS	LVDS	-0.15	-0.15	-0.15	ns
RSDS	RSDS	-0.15	-0.15	-0.15	ns
LVPECL33	LVPECL	0.16	0.15	0.13	ns
HSTL18_I	HSTL_18 class I	0.01	-0.01	-0.04	ns
HSTL18_II	HSTL_18 class II	0.01	-0.01	-0.04	ns
HSTL18D_I	Differential HSTL 18 class I	0.01	-0.01	-0.04	ns
HSTL18D_II	Differential HSTL 18 class II	0.01	-0.01	-0.04	ns
HSTL15_I	HSTL_15 class I	0.01	-0.01	-0.04	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	-0.01	-0.04	ns
SSTL33_I	SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33_II	SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL33D_I	Differential SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33D_II	Differential SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL25_I	SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25_II	SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25D_II	Differential SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL18_I	SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18_II	SSTL_18 class II	-0.01	-0.04	-0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18D_II	Differential SSTL_18 class II	-0.01	-0.04	-0.07	ns
LVTTL33	LVTTL	-0.16	-0.16	-0.16	ns
LVCMOS33	LVCMOS 3.3	-0.08	-0.12	-0.16	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.16	-0.17	-0.17	ns
LVCMOS15	LVCMOS 1.5	-0.14	-0.14	-0.14	ns
LVCMOS12	LVCMOS 1.2	-0.04	-0.01	0.01	ns
PCI33	PCI	-0.08	-0.12	-0.16	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E[4]	0.25	0.19	0.13	ns
LVDS25	LVDS 2.5	0.10	0.13	0.17	ns
BLVDS25	BLVDS 2.5	0.00	-0.01	-0.03	ns
MLVDS	MLVDS 2.5[4]	0.00	-0.01	-0.03	ns
RSDS	RSDS 2.5[4]	0.25	0.19	0.13	ns
LVPECL33	LVPECL 3.3[4]	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18_II	HSTL_18 class II	-0.30	-0.34	-0.37	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.22	-0.25	ns

LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.34	-0.37	ns
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTL33_4mA	LVTTL 4mA drive	0.52	0.60	0.68	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.08	0.09	ns
LVTTL33_12mA	LVTTL 12mA drive	0.04	0.04	0.05	ns
LVTTL33_16mA	LVTTL 16mA drive	0.03	0.02	0.02	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns

LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	2.18	2.26	2.33	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	2.19	2.35	2.51	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.50	1.66	1.82	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.60	1.59	1.58	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.43	1.39	1.34	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	2.22	2.27	2.32	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.93	2.08	2.23	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.43	1.51	1.58	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.47	1.46	1.45	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	2.32	2.38	2.43	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	1.84	1.98	2.12	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	2.52	2.63	2.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	1.69	1.83	1.96	ns
PCI33	PCI33	0.04	0.04	0.04	ns

1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.

Timing v.A 0.10

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor[5, 6]	2	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	25	—	420	MHz
		With external capacitor[5]	5	—	50	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.195	—	210	MHz
		With external capacitor[5]	0.039	—	25	MHz
f_{VCO}	PLL VCO Frequency		640	—	1280	MHz
f_{PFD}	Phase Detector Input Frequency	Without external capacitor	25	—	420	MHz
		With external capacitor[5, 6]	2	—	50	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	±0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	—	±125	ps
		$50 \leq f_{OUT} < 100$ MHz	—		0.025	UIPP
		$f_{OUT} < 50$ MHz	—	—	0.04	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—	150	µs
		With external capacitor[5]	—	—	500	µs
t_{PA}	Programmable Delay Unit		85	130	360	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor[5]	20	—	—	µs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. f_{OUT} (max) = f_{IN} * 10 for f_{IN} < 5MHz.

Timing v.A 0.10

sysCLOCK SPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	33	—	420	MHz
		With external capacitor[5, 6]	2	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	33	—	420	MHz
		With external capacitor[5]	5	—	50	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.258	—	210	MHz
		With external capacitor[5]	0.039	—	25	MHz
f_{VCO}	PLL VCO Frequency		640	—	1280	MHz
f_{PFD}	Phase Detector Input Frequency	Without external capacitor	33	—	420	MHz
		With external capacitor[6]	2	—	50	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Selected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	±0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	—	±125	ps
		$50 \leq f_{OUT} < 100$ MHz	—	—	0.025	UIPP
		$f_{OUT} < 50$ MHz	—	—	0.04	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider Ratio = Integer	—	—	±250	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—	150	µs
		With external capacitor[5]	—	—	500	µs
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor[5]	20	—	—	µs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Phase accuracy of CLKOS compared to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. f_{OUT} (max) = f_{IN} * 10 for f_{IN} < 5MHz.

Timing v.A 0.10

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP	100	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS	25	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)		—	250	ps p-p
t_{CYJIT}	Output clock cycle to cycle jitter (clean input)			250	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	35		65	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	40		60	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode)	40		60	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting	—	—	100	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)	750	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)	750	—	—	ps
t_R, t_F	Input clock rise and fall time (20% to 80% levels)	—	—	1	ns
t_{INSTB}	Input clock period jitter	—	—	+/-250	ps
t_{LOCK}	DLL lock time	18,500	—	—	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)	3	—	—	ns
t_{PA}	Delay step size	16.5	42	59.4	ps
t_{RANGE1}	Max. delay setting for single delay block (144 taps)	2.376	6	8.553	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks	9.504	24	34.214	ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

Timing v.A 0.10

SERDES High Speed Data Transmitter[1] (LatticeECP2M Family Only)

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.25}$	Differential swing (1.25V setting)[1, 2]	0.25 to 3.125 Gbps	—	1.25		V, p-p
$V_{TX-DIFF-P-P-1.4}$	Differential swing (1.4V setting)[1, 2]	0.25 to 3.125 Gbps	—	1.4		V, p-p
$V_{TX-DIFF-P-P-1.0}$	Differential swing (1.0V setting)[1, 2]	0.25 to 3.125 Gbps	—	1.0		V, p-p
$V_{TX-DIFF-P-P-1.2}$	Differential swing (1.2V setting)[1, 2]	0.25 to 3.125 Gbps	—	1.2		V, p-p
V_{OCM}	Output common mode voltage	—	—	0.8		V
T_{TX-R}	Rise time (20% to 80%)	—	—	70		ps
T_{TX-F}	Fall time (80% to 20%)	—	—	70		ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ K Ohms (single ended)	—	—	50/75/ HiZ		Ohms
R_{LTX-RL}	Return loss (with package)	—	—	9		dB

1. All measurements are with 50 ohm impedance.
2. See technical note TN1124, *LatticeECP2/M SERDES/PCS Usage Guide* for actual binary settings and the min-max range.

Table 3-8. Channel Output Jitter

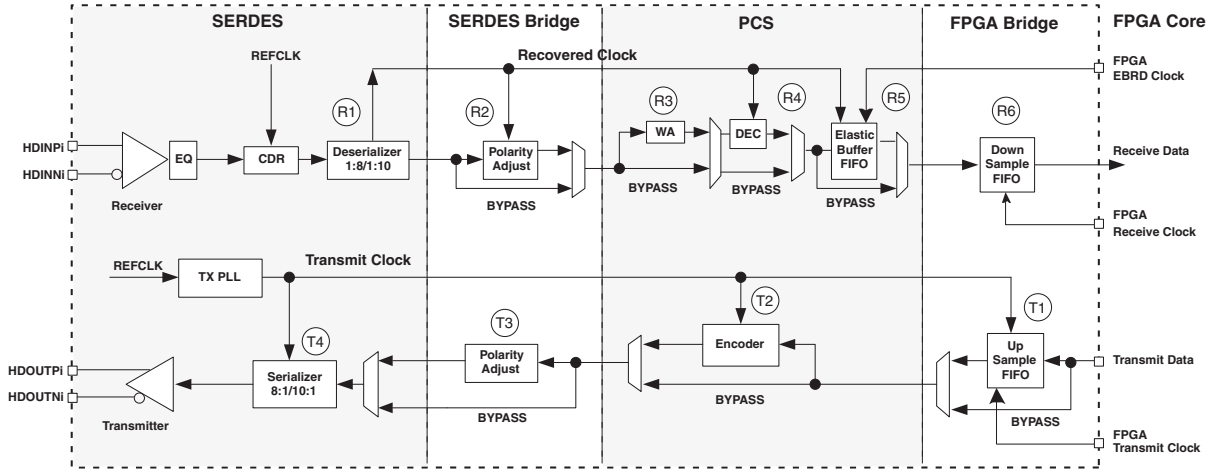
Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.08	UI, p-p
Random	3.125 Gbps	—	0.22	0.33	UI, p-p
Total	3.125 Gbps	—	0.33	0.41	UI, p-p
Deterministic	2.5Gbps	—	0.05	0.09	UI, p-p
Random	2.5Gbps	—	0.17	0.30	UI, p-p
Total	2.5Gbps	—	0.24	0.34	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.03	UI, p-p
Random	1.25 Gbps	—	0.10	0.17	UI, p-p
Total	1.25 Gbps	—	0.15	0.18	UI, p-p
Deterministic	250 Mbps	—	0.04	0.04	UI, p-p
Random	250 Mbps	—	0.12	0.17	UI, p-p
Total	250 Mbps	—	0.15	0.18	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

Table 3-9. SERDES/PCS Latency Breakdown (Parallel Clock Cycle)

Item	Description	Min.	Average	Max.	Bypass
Transmit Data Latency					
T1	FPGA Bridge Transmit	1	3	5	1
T2	8b10b Encoder	2	2	2	1
T3	SERDES Bridge Transmit	2	2	2	1
T4	Serializer			2.4	
Receive Data Latency					
R1	Deserializer			1.2	
R2	SERDES Bridge Receive	2	2	2	1
R3	Word Alignment	4	4	4	0
R4	8b10b Decoder	1	1	1	1
R5	Clock Tolerance Compensation	7	15	23	1
R6	FPGA Bridge Receive	1	3	5	1

Figure 3-13. Transmitter and Receiver Block Diagram



SERDES High Speed Data Receiver (LatticeECP2M Family Only)

Table 3-10. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER		7 @ 3.125 Gbps 20 @ 1.25 Gbps		Bits
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity	100	—	—	mV, p-p
$V_{RX\text{-}IN}$	Input levels	0	—	V_{CCRX} + 0.3	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)	0.5	—	1.2	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]	0	—	1.5	V
$T_{RX\text{-}RELOCK}$	CDR re-lock time[2]	—	3000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z	—	50		Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)	—	9	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-11. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.54	UI, p-p
Random		600 mV differential eye	—	—	0.26	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.61	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.81	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.53	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	250 Gbps	600 mV differential eye	—	—		UI, p-p
Random		600 mV differential eye	—	—		UI, p-p
Total		600 mV differential eye	—	—		UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Table 3-12. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	3.125 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.25 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
Periodic	250 Gbps	600 mV differential eye	—	—		UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating.

SERDES External Reference Clock (LatticeECP2M Family Only)

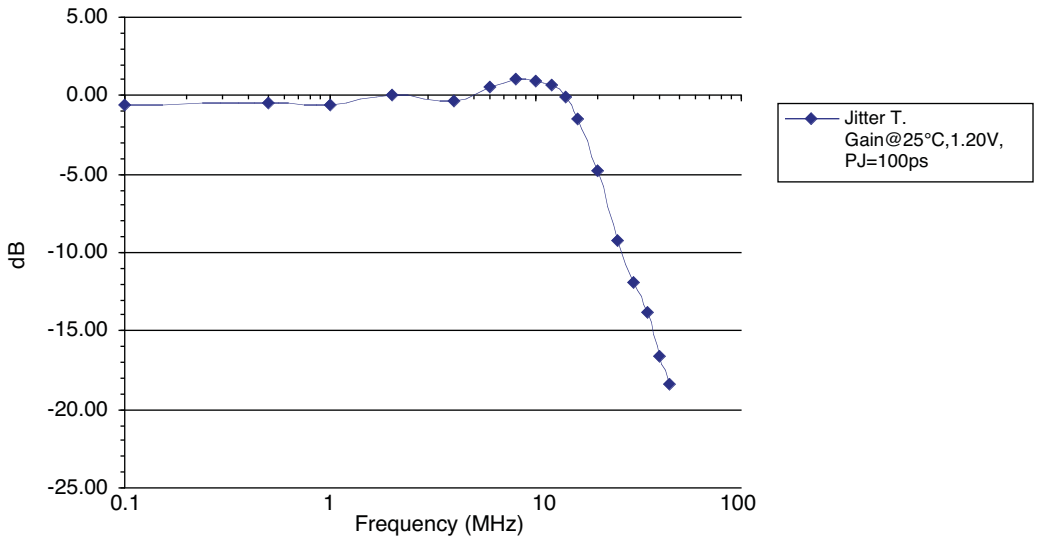
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-13 specifies reference clock requirements, over the full range of operating conditions.

Table 3-13. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	25	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance	-300	—	300	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[1]	100	—	1200	mV, p-p
V_{REF-IN}	Input levels	0	—	V_{CCRX} + 0.3	V
$V_{REF-CM-DC}$	Input common mode range (DC coupled)	0.5	—	1.2	V
$V_{REF-CM-AC}$	Input common mode range (AC coupled)[2]	0	—	1.5	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)		500	1000	ps
T_{REF-F}	Fall time (80% to 20%)		500	1000	ps
$Z_{REF-IN-TERM}$	Input termination		50/2K		Ohms
$C_{REF-IN-CAP}$	Input capacitance[4]	—	—	1.5	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
(Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

Figure 3-14. Jitter Transfer



Note: This graph is for a nominal device.

SERDES Power-Down/Power-Up Specification

Table 3-14. Power-Down and Power-Up Specification

Symbol	Description	Max.	Units
t_{PWRDN}	Power-down time after all power down register bits set to '0'	10	s
t_{PWRUP}	Power-up time after all power down register bits set to '1'	5	ms

PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit[1, 2]

Symbol	Description	Test Conditions	Min	Typ	Max	Units
UI	Unit interval		399.88	400	400.12	ps
$V_{TX-DIFF\_P-P}$	Differential peak-to-peak output voltage		0.8	1.0	1.2	V
$V_{TX-DE-RATIO}$	De-emphasis differential output voltage ratio		0	-3.5	-7.96	dB
$V_{TX-CM-AC\_P}$	RMS AC peak common-mode output voltage		—	20	—	mV
$V_{TX-CM-DC-LINE-DELTA}$	Maximum Common mode voltage delta between n and p channels		—	—	25	mV
$V_{TX-DC-CM}$	Tx DC common mode voltage		0	—	V_{CCOB} + 5%	V
$I_{TX-SHORT}$	Output short circuit current	V_{TX-D+}=0.0V V_{TX-D-}=0.0V	—	—	90	mA
$Z_{TX-DIFF-DC}$	Differential output impedance		80	100	120	Ohms
$T_{TX-RISE}$	Tx output rise time	20 to 80%	0.125	—	—	UI
$T_{TX-FALL}$	Tx output fall time	20 to 80%	0.125	—	—	UI
$L_{TX-SKEW}$	Lane-to-lane static output skew for all lanes in port/link		—	—	1.3	ns
T_{TX-EYE}	Transmitter eye width		0.75	—	—	UI
$T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$[3]			—	—	0.125	UI
C_{TX}	AC coupling capacitor		75	—	200	nF

1. Values are measured at 2.5 Gbps.
2. Compliant to PCI Express v1.1.
3. Measured at 60ps with plug-in board and jitter due to socket removed.

Table 3-16. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
UI	Unit Interval		399.88	400	400.12	ps
$V_{RX-DIFF\_P-P}$	Differential peak-to-peak input voltage		0.175	—	—	V
$V_{RX-IDLE-DET-DIFF\_P-P}$	Idle detect threshold voltage		65	—	175	mV
$Z_{RX-DIFF-DC}$	DC differential input impedance		80	100	120	Ohms
Z_{RX-DC}	DC input impedance		40	50	60	Ohms
$Z_{RX-HIGH-IMP-DC}$[1]	Power-down DC input impedance		200K	—	—	Ohms
T_{RX-EYE}	Receiver eye width		0.4	—	—	UI
$T_{RX-EYE-MEDIAN-TO-MAX-JITTER}$			—	—	0.3	UI

Notes:
1. Measured with external AC-coupling on the receiver
2. Values are measured at 2.5 Gbps

Table 3-17. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{REFCLK}	Reference clock frequency		—	100	—	MHz
V_{CM}	Input common mode voltage		—	0.65	—	V
T_R/T_F	Clock input rise/fall time		—	—	1.0	ns
V_{SW}	Differential input voltage swing		0.6	—	1.6	V
DC_{REFCLK}	Input clock duty cycle		40	50	60	%
PPM	Reference clock tolerance		-300	—	+300	ppm

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUMCDI}	DI Setup Time to CCLK Master Mode	7	—	ns
t_{HMCDI}	DI Hold Time to CCLK Master Mode	1	—	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	50	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay	—	1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CCLK Low	—	1	µs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LatticeECP2/M sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

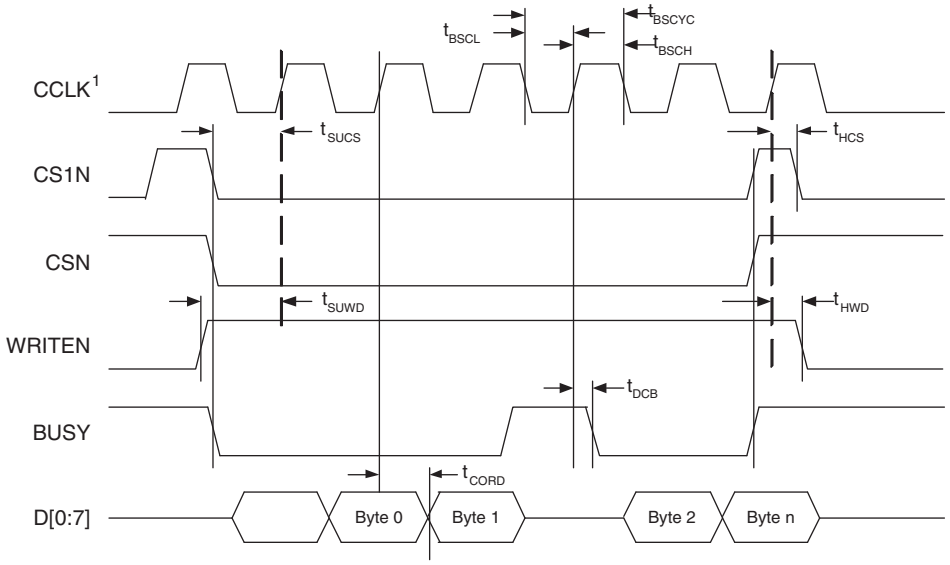
Parameter	Description	Min.	Max.	Units
f_{MAXSPI}	Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1)	—	20	MHz
	Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0)	—	50	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	2	—	ns

Timing v.A 0.10

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
Duty Cycle	40	60	%

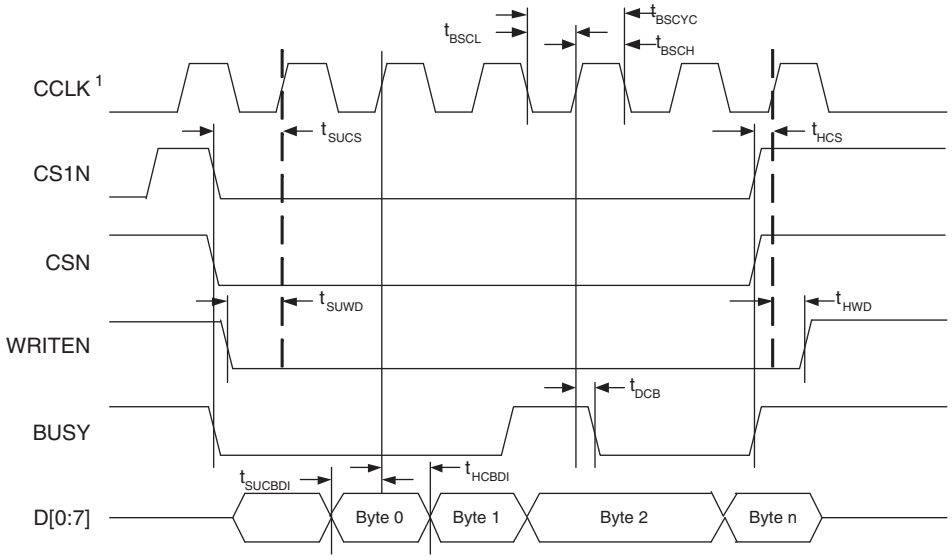
Timing v.A 0.10

Figure 3-15. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-16. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-17. sysCONFIG Master Serial Port Timing

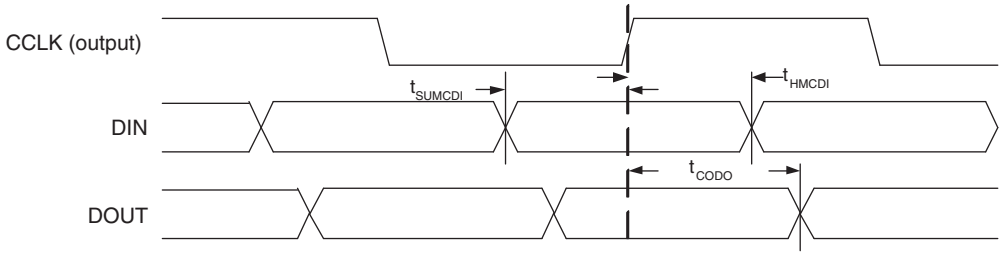


Figure 3-18. sysCONFIG Slave Serial Port Timing

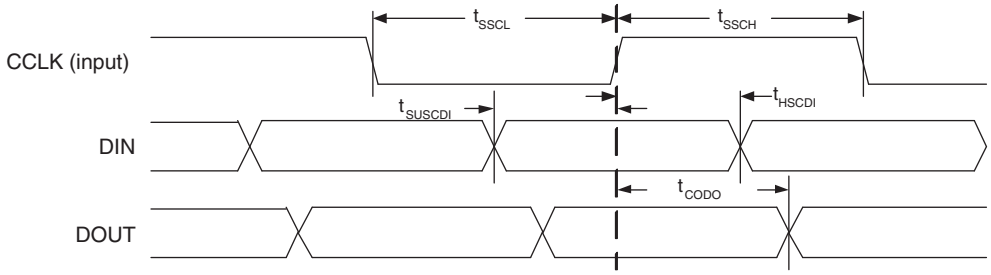
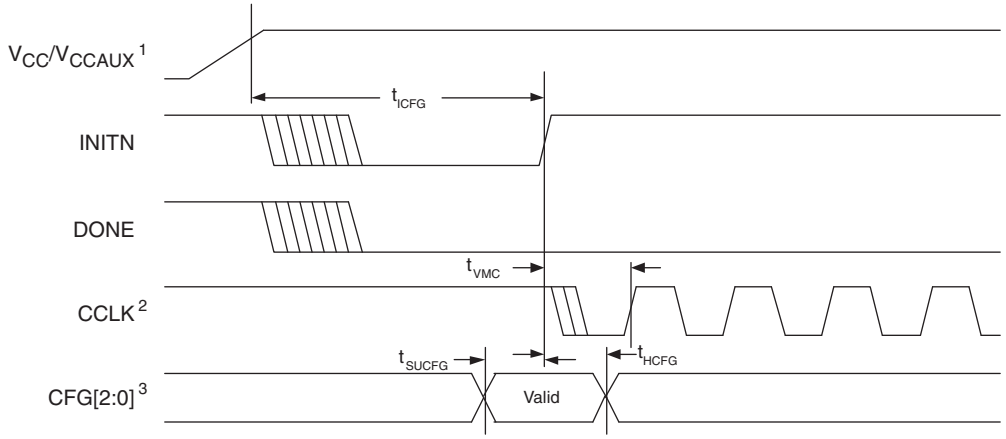
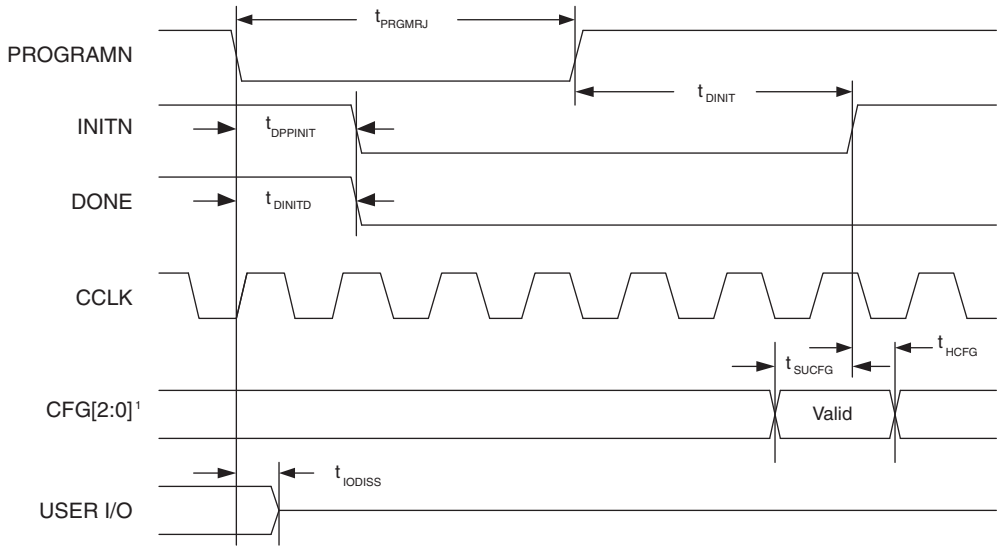


Figure 3-19. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX}, whichever is the last to reach its V_{MIN}.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

Figure 3-20. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-21. Wake-Up Timing

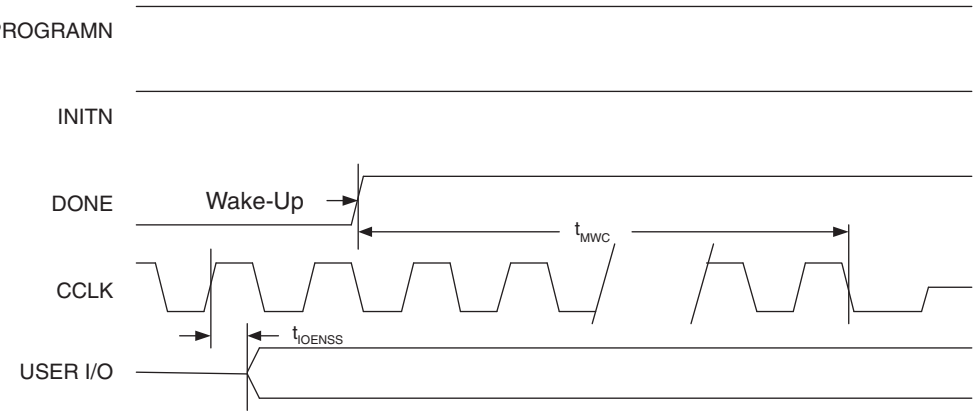
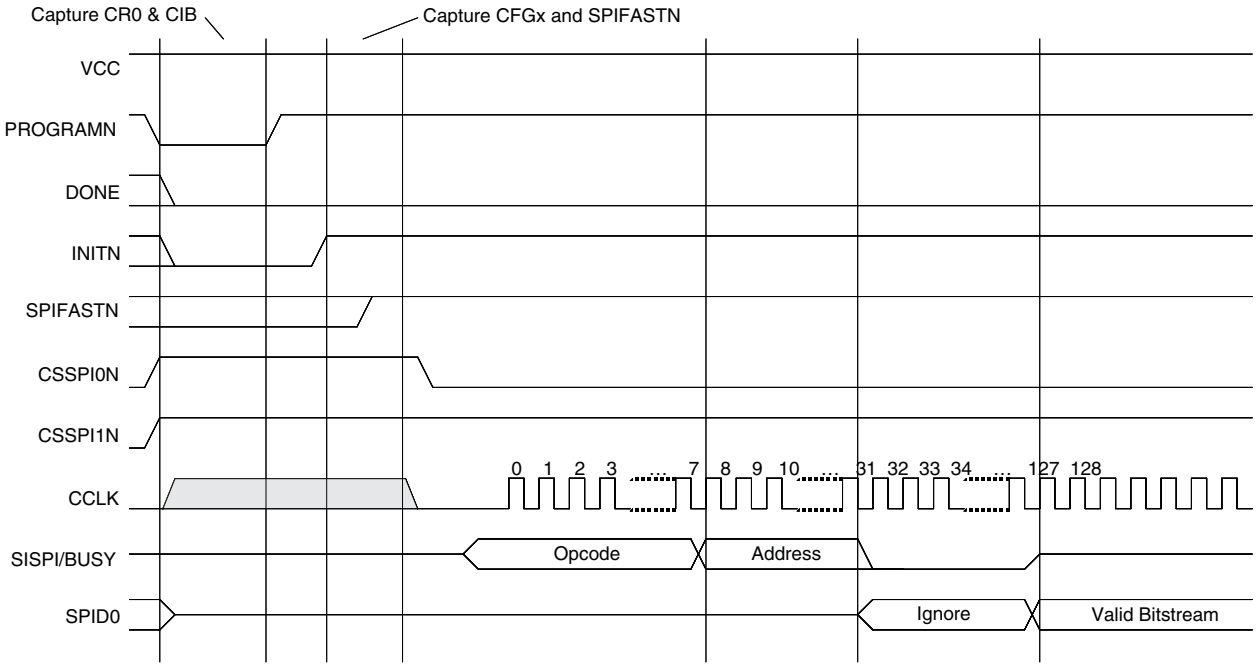


Figure 3-22. SPI/SPIm Configuration Waveforms



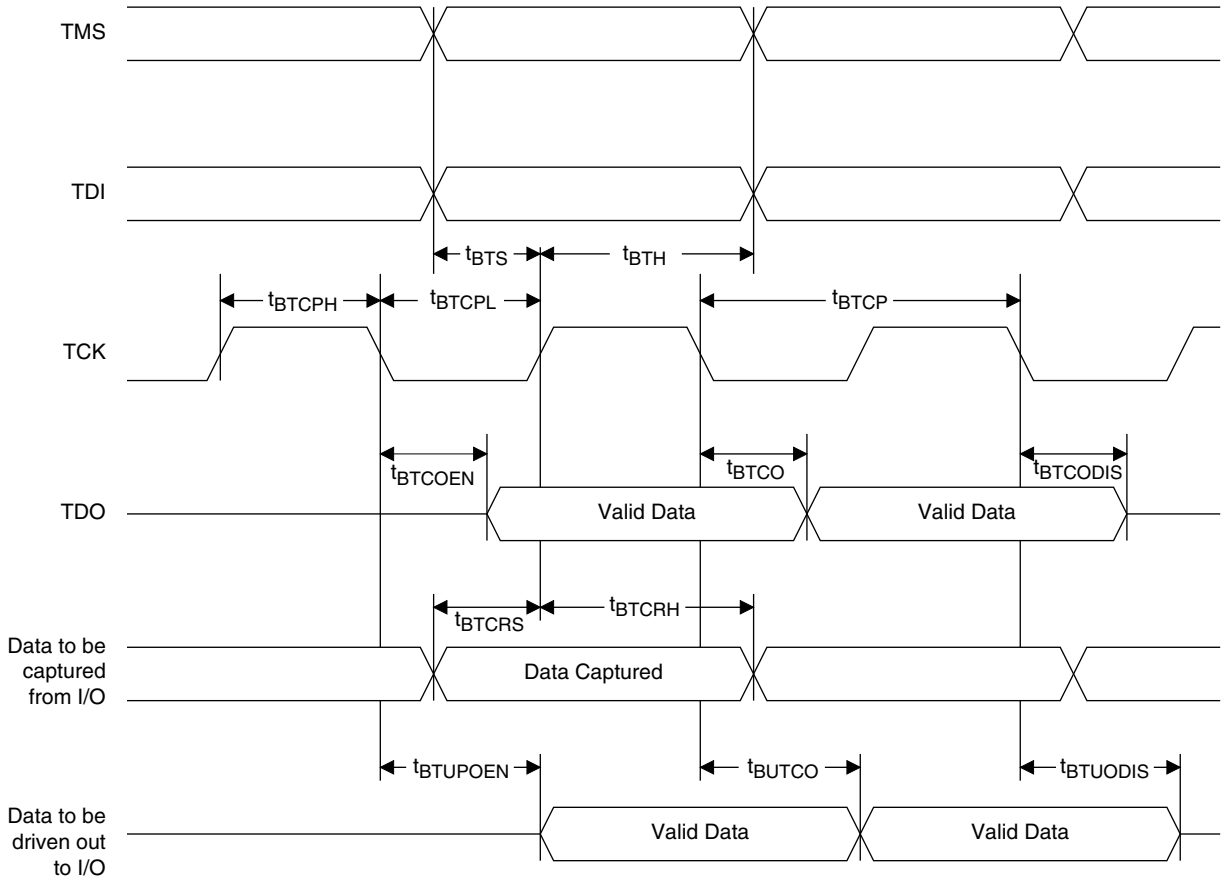
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.A 0.10

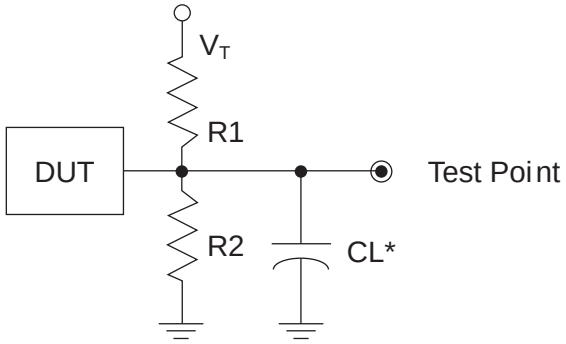
Figure 3-23. JTAG Port Timing Waveforms



Switching Test Conditions

Figure 3-24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-18.

Figure 3-24. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-18. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name[1, 2, 3]	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
XRES[4]	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP[4]	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V_{CCPLL}	—	Power supply pin for PLL: ULM, LLM, URM, LRM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A	I	Secondary PLL (SPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A	I	Optional feedback (SPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.

Signal Descriptions (Cont.)

Signal Name[1, 2, 3]	I/O	Description
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSON (for LatticeECP2 only) DOUT/CSON/CSSPI1N (for LatticeECP2M)	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. CSSPI1N is used in SPIm Mode only.
DI/CSSPI0N	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes.
Dedicated SERDES Signals		
[LOC]_SQ_VCCAUX33	—	Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused.
[LOC]_SQ_REFCLKN	I	Negative Reference Clock Input
[LOC]_SQ_REFCLKP	I	Positive Reference Clock Input
[LOC]_SQ_VCCP	—	PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused.
[LOC]_SQ_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_HDOUTNm	O	High-speed output, negative channel m
[LOC]_SQ_HDOUTPm	O	High-speed output, positive channel m
[LOC]_SQ_HDINNm	I	High-speed input, negative channel m

Signal Descriptions (Cont.)

Signal Name[1, 2, 3]	I/O	Description
[LOC]_SQ_HDINPm	I	High-speed input, positive channel m
[LOC]_SQ_VCCTXm[4]	—	Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.
[LOC]_SQ_VCCRXm[4]	—	Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to technical note TN1159, *LatticeECP2/M Pin Assignment Recommendations*.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Bottom Edge of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Single Ended User I/O		90	190	93	131	193	297
Differential Pair User I/O		43	95	45	62	96	148
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	34	54	33	40	54	57
	Dedicated Pins	3	3	3	3	3	3
VCC		10	7	10	14	7	16
VCCAUX		4	4	4	8	4	16
VCCPLL		0	0	0	0	0	0
VCCIO	Bank0	1	2	1	2	2	4
	Bank1	1	2	1	2	2	4
	Bank2	1	2	1	2	2	4
	Bank3	1	2	1	2	2	4
	Bank4	1	2	1	2	2	4
	Bank5	1	2	1	2	2	4
	Bank6	1	2	1	2	2	4
	Bank7	1	2	1	2	2	4
	Bank8	1	1	1	2	1	2
GND, GND0 to GND7		12	20	12	22	20	60
NC		4	3	1	0	0	44
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	8/4	18/6	8/4	18/9	18/9	50/25
	Bank1	17/8	34/17	18/9	18/9	34/17	46/23
	Bank2	4/2	20/10	4/2	11/5	20/10	24/12
	Bank3	8/4	12/6	8/4	11/5	12/6	16/8
	Bank4	18/9	32/16	18/9	19/9	32/16	46/23
	Bank5	8/4	14/7	10/5	18/9	17/8	46/23
	Bank6	9/4	26/13	9/4	18/8	26/13	32/16
	Bank7	12/6	20/10	12/6	12/6	20/10	23/11
	Bank8	6/2	14/7	6/2	6/2	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	1	5	1	4	5	6
	Bank3 (Right Edge)	3	3	3	3	3	4
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	2	7	2	6	7	8
	Bank7 (Left Edge)	5	5	5	5	5	5
	Bank8 (Right Edge)	0	0	0	0	0	0

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		131	193	331	402	331	450
Differential Pair User I/O		62	96	165	200	165	224
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	42	54	60	64	60	68
	Dedicated Pins	3	3	3	3	3	3
VCC		14	7	18	24	16	22
VCCAUX		8	4	16	16	16	16
VCCPLL		0	0	0	0	2	2
VCCIO	Bank0	2	2	4	5	4	5
	Bank1	2	2	4	5	4	5
	Bank2	2	2	4	5	4	5
	Bank3	2	2	4	5	4	5
	Bank4	2	2	4	5	4	5
	Bank5	2	2	4	5	4	5
	Bank6	2	2	4	5	4	5
	Bank7	2	2	4	5	4	5
	Bank8	2	1	2	2	2	2
GND, GND0 to GND7		22	20	60	72	60	72
NC		0	1	8	101	8	102
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	18/9	18/9	50/25	67/33	50/25	67/33
	Bank1	18/9	34/17	46/23	52/26	46/23	52/26
	Bank2	11/5	20/10	34/17	36/18	34/17	48/24
	Bank3	11/5	12/6	22/11	32/16	22/11	42/21
	Bank4	19/9	32/16	46/23	50/25	46/23	54/27
	Bank5	18/9	17/8	46/23	68/34	46/23	68/34
	Bank6	18/8	26/13	40/20	48/24	40/20	58/29
	Bank7	12/6	20/10	33/16	35/17	33/16	47/23
	Bank8	6/2	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	4	5	9	9	9	12
	Bank3 (Right Edge)	3	3	5	8	5	9
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	6	7	10	12	10	13
	Bank7 (Left Edge)	5	5	8	8	8	11
	Bank8 (Right Edge)	0	0	0	0	0	0

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Single Ended User I/O		339	500	500	583
Differential Pair User I/O		169	249	249	290
Configuration	TAP Pins	5	5	5	5
	Muxed Pins	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7
Non Configuration	Muxed Pins	68	79	79	89
	Dedicated Pins	3	3	3	3
VCC		16	20	20	26
VCCAUX		16	16	16	17
VCCPLL		4	4	2	4
VCCIO	Bank0	4	5	5	6
	Bank1	4	5	5	6
	Bank2	4	5	5	6
	Bank3	4	5	5	6
	Bank4	4	5	5	6
	Bank5	4	5	5	6
	Bank6	4	5	5	6
	Bank7	4	5	5	6
	Bank8	2	2	2	2
GND, GND0 to GND7		61	72	72	104
NC		0	3	5	101
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	50/25	67/33	67/33	84/42
	Bank1	46/23	66/33	66/33	76/38
	Bank2	38/19	56/28	56/28	74/37
	Bank3	22/11	48/24	48/24	48/24
	Bank4	46/23	62/31	62/31	72/35
	Bank5	46/23	68/34	68/34	80/40
	Bank6	40/20	64/32	64/32	64/32
	Bank7	37/18	55/27	55/27	71/35
	Bank8	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0
	Bank2 (Right Edge)	9	13	13	18
	Bank3 (Right Edge)	5	12	12	12
	Bank4 (Bottom Edge)	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0
	Bank6 (Left Edge)	10	16	16	16
	Bank7 (Left Edge)	8	12	12	16
	Bank8 (Right Edge)	0	0	0	0

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70 (Cont.)

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	2	3	3	4
	Bank3	0	3	3	3
	Bank4	3	4	4	4
	Bank5	3	4	4	5
	Bank6	1	4	4	4
	Bank7	2	3	3	4
	Bank8	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	0	0	0	0
	Bank3	0	0	0	0
	Bank4	46	62	62	72
	Bank5	46	68	68	80
	Bank6	0	0	0	0
	Bank7	0	0	0	0
	Bank8	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Pin Information Summary

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

LatticeECP2M Pin Information Summary (Cont.)

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0	0
	Bank1	0	0	0	0	0
	Bank2	0	2	0	1	3
	Bank3	0	4	0	0	2
	Bank4	2	4	2	4	3
	Bank5	1	2	1	2	3
	Bank6	0	3	0	1	2
	Bank7	1	2	1	2	3
	Bank8	0	0	0	11	16
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0
	Bank1	0	0	0	0	0
	Bank2	0	0	0	0	0
	Bank3	0	0	0	0	0
	Bank4	32	62	32	62	50
	Bank5	20	28	20	28	60
	Bank6	16	40	16	39	52
	Bank7	28	40	28	40	60
	Bank8	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Available Device Resources by Package, LatticeECP2

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA
PLL/DLL	ECP2-6	4	—	—	—
	ECP2-12	4	4	—	—
	ECP2-20	4	4	4	—
	ECP2-35	—	4	4	—
	ECP2-50	—	6	6	—
	ECP2-70	—	—	8	8

Available Device Resources by Package, LatticeECP2M

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA	1152 fpBGA	1156 fpBGA
PLL/DLL	ECP2M20	10	10	—	—	—	—
	ECP2M35	10	10	10	—	—	—
	ECP2M50	—	10	10	10	—	—
	ECP2M70	—	—	—	10	10	—
	ECP2M100	—	—	—	10	10	10

LatticeECP2 Power Supply and NC

Signals	144 TQFP[3]	208 PQFP[3]	256 fpBGA[4]	484 fpBGA[4]
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	**LFE2-6:** G7, G9, G10, H7, J10, K10, K8 **LFE2-12/LFE2-20:** G7, G9, G10, H7, J10, K10, K8	**LFE2-12/LFE2-20:** N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 **LFE2-35/LFE2-50:** J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	**LFE2-12/LFE2-20:** None **LFE2-35:** N6, N18 **LFE2-50:** N6, N18, K6, J16
GND[1]	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC[2]	**LFE2-6:** 45, 46, 124, 127 **LFE2-12:** 127	None	**LFE2-6:** K6, R3, P4 **LFE2-12/LFE2-20:** None	**LFE2-12:** E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-20/LFE2-35:** K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-50:** None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LatticeECP2 Power Supply and NC (Cont.)

Signals	672 fpBGA[3]	900 fpBGA[3]
VCC	**LFE2-20:** R8, P18, M8, L20, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 **LFE2-35/LFE2-50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 **LFE2-70:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	AA11, AA20, K11, K21, K22, L11, L12, L13, L18, L19, L20, M11, M20, N11, N20, V11, V20, W11, W20, Y10, Y11, Y12, Y13, Y18, Y19, Y20
VCCIO0	D11, D6, G9, J12, K12	J13, J14, K12, K13, K14, K15
VCCIO1	D16, D21, G18, J15, K15	J17, J18, J20, K17, K18, K20
VCCIO2	F23, J20, L23, M17, M18	L21, M21, M22, N21, N22, R21
VCCIO3	AA23, R17, R18, T23, V20	U21, U22, V21, V22, W21, Y22
VCCIO4	AC16, AC21, U15, V15, Y18	AA16, AA17, AA18, AA19, AB17, AB18
VCCIO5	AC11, AC6, U12, V12, Y9	AA12, AA13, AA14, AB12, AB13, AB14
VCCIO6	AA4, R10, R9, T4, V7	U10, U9, V10, W10, W9, Y9
VCCIO7	F4, J7, L4, M10, M9	L10, L9, M10, N10, P10, R10
VCCIO8	AE25, V18	AA21, Y21
VCCJ	AB5	AD3
VCCAUX	J10, J11, J16, J17, K18, L18, T18, U18, V16, V17, V10, V11, T9, U9, K9, L9	AA15, AB11, AB19, AB20, J11, J12, J19, K19, L22, M9, N9, P21, P9, T10, T21, V9, W22
VCCPLL	**LFE2-20:** None **LFE2-35/LFE2-70:** R8, P18 **LFE2-50:** R8, P18, M8, L20	P22, P8, T22, Y7
GND[1]	A2, A25, AA18, AA24, AA3, AA9, AD11, AD16, AD21, AD6, AE1, AE26, AF2, AF25, B1, B26, C11, C16, C21, C6, F18, F24, F3, F9, J13, J14, J21, J6, K10, K11, K13, K14, K16, K17, L10, L11, L16, L17, L24, L3, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T24, T3, U10, U11, U13, U14, U16, U17, V13, V14, V21, V6	A1, A30, AC28, AC3, AH13, AH18, AH23, AH28, AH3, AH8, AK1, AK30, C13, C18, C23, C28, C3, C8, H28, H3, L14, L15, L16, L17, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, N28, N3, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V12, V13, V14, V15, V16, V17, V18, V19, V28, V3, W12, W13, W14, W15, W16, W17, W18, W19, Y14, Y15, Y16, Y17
NC[2]	**LFE2-20:** E4, E3, E2, E1, H6, H5, F2, F1, H8, J9, G4, G3, K3, K2, K1, L2, L1, M2, M1, N2, T1, T2, P8, P6, P5, P4, U1, V1, P3, R3, R4, U2, V2, W2, T6, R5, AA19, W17, Y19, Y17, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, R22, T21, P26, P25, R24, R23, P20, R19, P21, P19, P23, P22, N22, R21, N26, N25, J26, J25, J23, K23, H26, H25, H24, H23, F22, E24, D25, C25, D24, B25, H21, G22, B24, C24, D23, C23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24 **LFE2-35:** K3, K2, K1, L2, L1, M2, M1, N2, M8, P3, R3, R4, U2, V2, W2, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, P26, P25, R24, R23, P20, R19, L20, J26, J25, J23, K23, H26, H25, H24, H23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24 **LFE2-50:** N6, P24, M3 **LFE2-70:** M8, L20, M3, P24, N6	A2, A3, A4, A5, AB28, AC4, AD23, AE1, AE2, AE29, AE3, AE30, AE4, AE5, AE6, AF1, AF2, AF23, AF26, AF27, AF28, AF29, AF3, AF30, AF4, AF5, AG1, AG13, AG16, AG18, AG2, AG26, AG27, AG28, AG29, AG3, AG30, AG4, AG8, AH1, AH16, AH2, AH26, AH27, AH29, AH30, AH4, AJ1, AJ2, AJ27, AJ28, AJ29, AJ3, AJ30, AK2, AK27, AK28, AK29, AK3, B1, B2, B3, B30, B4, B5, C1, C2, C29, C30, C4, D13, D18, D23, D28, D29, D3, D30, D4, E25, E26, E27, E28, E29, E3, E30, E4, E5, E6, F25, F5, F6, G6, G7, K10, K9, N27, N4, R1, R2, V27, V4

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LatticeECP2M Power Supply and NC

Signal	256 fpBGA	484 fpBGA	672 fpBGA
V_{CC}	G7, G9, H7, J10, K10, K8	J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13	**LFE2M35:** AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15
V_{CCIO0}	E7	B5, B9, E7, H9	B12, B7, F11, J13, K12
V_{CCIO1}	E10	D13, E16, H14	D18, F16, J14, K15
V_{CCIO2}	E14, G12	E21, G18, J15, K19	G25, L21, M17, M25, N18
V_{CCIO3}	K12, M14	N19, P15, T18, V21	P18, R17, R25, T21, Y25
V_{CCIO4}	M10, P12	AA18, R14, V16, W13	AA16, AC18, U15, V14
V_{CCIO5}	M7, P5	AA5, R9, V7, W10	AA11, AE12, AE7, U12, V13
V_{CCIO6}	K5, M3	N4, P8, T5, V2	P9, R10, R2, T6, Y2
V_{CCIO7}	E3, G5	E2, G5, J8, K4	G2, L6, M10, M2, N9
V_{CCIO8}	T15	AA22, U19	AC24, U17
V_{CCJ}	K7	W4	AA7
V_{CCAUX}	G8, H10, J7, K9	H11, H12, L15, L8, M15, M8, R11, R12	**LFE2M35:** AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16
V_{CCPLL}	G10	R8, H15, H8, R15	H7, K6, P7, R8, V18, P20, J17, G19
SERDES Power[3]	C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3	C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10	**LFE2M35:** C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13
GND[1]	A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16
NC[2]	D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9	LFE2M20: D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15	**LFE2M35:** AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to technical note TN1160, *LatticeECP2/M Density Migration,* for more details.

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 144 TQFP

LFE2-6E/6-SE					LFE2-12E/12SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
1	PL2A	7	VREF2_7	T (LVDS)*	1	PL2A	7	VREF2_7	T (LVDS)*
2	PL2B	7	VREF1_7	C (LVDS)*	2	PL2B	7	VREF1_7	C (LVDS)*
3	PL4A	7		T (LVDS)*	3	PL4A	7		T (LVDS)*
4	PL4B	7		C (LVDS)*	4	PL4B	7		C (LVDS)*
5	PL6A	7		T (LVDS)*	5	PL6A	7		T (LVDS)*
6	VCCAUX	-			6	VCCAUX	-		
7	PL6B	7		C (LVDS)*	7	PL6B	7		C (LVDS)*
8	PL8A	7		T (LVDS)*	8	PL8A	7		T (LVDS)*
9	VCCIO7	7			9	VCCIO7	7		
10	PL8B	7		C (LVDS)*	10	PL8B	7		C (LVDS)*
11	GND	-			11	GND	-		
12	PL12A	7		T (LVDS)*	12	PL12A	7		T (LVDS)*
13	PL12B	7		C (LVDS)*	13	PL12B	7		C (LVDS)*
14	PL13A	7	PCLKT7_0	T	14	PL13A	7	PCLKT7_0	T
15	PL13B	7	PCLKC7_0	C	15	PL13B	7	PCLKC7_0	C
16	VCC	-			16	VCC	-		
17	PL15A	6	PCLKT6_0	T (LVDS)*	17	PL15A	6	PCLKT6_0	T (LVDS)*
18	PL15B	6	PCLKC6_0	C (LVDS)*	18	PL15B	6	PCLKC6_0	C (LVDS)*
19	PL16A	6	VREF2_6	T	19	PL16A	6	VREF2_6	T
20	PL16B	6	VREF1_6	C	20	PL16B	6	VREF1_6	C
21	GND	-			21	GND	-		
22	VCC	-			22	VCC	-		
23	PL18A	6	LLM0_GDLLT_FB_A	T	23	PL18A	6	LLM0_GDLLT_FB_A	T
24	PL18B	6	LLM0_GDLLC_FB_A	C	24	PL18B	6	LLM0_GDLLC_FB_A	C
25	LLM0_PLLCAP	6			25	LLM0_PLLCAP	6		
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
28	PL22A	6			28	PL22A	6		
29	VCC	-			29	VCC	-		
30	GND	-			30	GND	-		
31	VCCIO6	6			31	VCCIO6	6		
32	TCK	-			32	TCK	-		
33	TDI	-			33	TDI	-		
34	TDO	-			34	TDO	-		
35	VCCJ	-			35	VCCJ	-		
36	TMS	-			36	TMS	-		
37	PB2A	5	VREF2_5	T	37	PB2A	5	VREF2_5	T
38	PB2B	5	VREF1_5	C	38	PB2B	5	VREF1_5	C
39	VCCAUX	-			39	VCCAUX	-		
40	PB4A	5		T	40	PB6A	5	BDQS6	T
41	PB4B	5		C	41	PB6B	5		C
42	VCCIO5	5			42	VCCIO5	5		
43	PB6A	5	BDQS6	T	43	PB12A	5		T
44	PB6B	5		C	44	PB12B	5		C

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/6-SE					LFE2-12E/12SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
45	NC	5			45	PB16A	5		T
46	NC	5			46	PB16B	5		C
47	GND	-			47	GND	-		
48	VCC				48	VCC	-		
49	PB8A	5	PCLKT5_0	T	49	PB26A	5	PCLKT5_0	T
50	PB8B	5	PCLKC5_0	C	50	PB26B	5	PCLKC5_0	C
51	GND	-			51	GND	-		
52	PB13A	4	PCLKT4_0	T	52	PB31A	4	PCLKT4_0	T
53	PB13B	4	PCLKC4_0	C	53	PB31B	4	PCLKC4_0	C
54	VCC	-			54	VCC	-		
55	PB14A	4		T	55	PB34A	4		T
56	PB14B	4		C	56	PB34B	4		C
57	PB16A	4		T	57	PB40A	4		T
58	PB16B	4		C	58	PB40B	4		C
59	PB18A	4		T	59	PB44A	4		T
60	PB18B	4		C	60	PB44B	4		C
61	GND	-			61	GND	-		
62	PB20A	4		T	62	PB48A	4		T
63	PB20B	4		C	63	PB48B	4		C
64	VCCIO4	4			64	VCCIO4	4		
65	PB22A	4		T	65	PB50A	4		T
66	PB22B	4		C	66	PB50B	4		C
67	PB24A	4	BDQS24	T	67	PB52A	4		T
68	PB24B	4		C	68	PB52B	4		C
69	PB26A	4		T	69	PB54A	4		T
70	PB26B	4		C	70	PB54B	4		C
71	PB28A	4	VREF2_4	T	71	PB55A	4	VREF2_4	T
72	PB28B	4	VREF1_4	C	72	PB55B	4	VREF1_4	C
73	CFG1	8			73	CFG1	8		
74	CFG2	8			74	CFG2	8		
75	PROGRAMN	8			75	PROGRAMN	8		
76	INITN	8			76	INITN	8		
77	CFG0	8			77	CFG0	8		
78	CCLK	8			78	CCLK	8		
79	DONE	8			79	DONE	8		
80	PR29A	8	D0		80	PR29A	8	D0	
81	GND	-			81	GND	-		
82	PR26A	8	D6		82	PR26A	8	D6	
83	VCC	-			83	VCC	-		
84	PR25B	8	D7	C	84	PR25B	8	D7	C
85	VCCIO8	8			85	VCCIO8	8		
86	PR25A	8	DI/CSSPI0N	T	86	PR25A	8	DI/CSSPI0N	T
87	PR24B	8	DOUT/CSON	C	87	PR24B	8	DOUT/CSON	C
88	PR24A	8	BUSY/SISPI	T	88	PR24A	8	BUSY/SISPI	T

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/6-SE					LFE2-12E/12SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
89	VCCIO3	3			89	VCCIO3	3		
90	VCCAUX	-			90	VCCAUX	-		
91	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	91	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
92	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	92	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
93	RLM0_PLLCAP	3			93	RLM0_PLLCAP	3		
94	VCC	-			94	VCC	-		
95	GND	-			95	GND	-		
96	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	96	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
97	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	97	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
98	PR16B	3	VREF2_3	C	98	PR16B	3	VREF2_3	C
99	PR16A	3	VREF1_3	T	99	PR16A	3	VREF1_3	T
100	PR15B	3	PCLKC3_0	C (LVDS)*	100	PR15B	3	PCLKC3_0	C (LVDS)*
101	PR15A	3	PCLKT3_0	T (LVDS)*	101	PR15A	3	PCLKT3_0	T (LVDS)*
102	VCC	-			102	VCC	-		
103	PR13B	2	PCLKC2_0	C	103	PR13B	2	PCLKC2_0	C
104	PR13A	2	PCLKT2_0	T	104	PR13A	2	PCLKT2_0	T
105	GND	-			105	GND	-		
106	VCCIO2	2			106	VCCIO2	2		
107	PR2B	2	VREF2_2	C (LVDS)*	107	PR2B	2	VREF2_2	C (LVDS)*
108	PR2A	2	VREF1_2	T (LVDS)*	108	PR2A	2	VREF1_2	T (LVDS)*
109	PT28B	1	VREF2_1	C	109	PT55B	1	VREF2_1	C
110	PT28A	1	VREF1_1	T	110	PT55A	1	VREF1_1	T
111	PT26B	1		C	111	PT54B	1		C
112	PT26A	1		T	112	PT54A	1		T
113	PT24B	1		C	113	PT52B	1		C
114	PT24A	1		T	114	PT52A	1		T
115	PT22B	1		C	115	PT50B	1		C
116	PT22A	1		T	116	PT50A	1		T
117	VCCIO1	1			117	VCCIO1	1		
118	PT20B	1		C	118	PT48B	1		C
119	PT20A	1		T	119	PT48A	1		T
120	GND	-			120	GND	-		
121	PT18B	1		C	121	PT44B	1		C
122	PT18A	1		T	122	PT44A	1		T
123	PT16A	1			123	PT40B	1		C
124	NC	1			124	PT40A	1		T
125	PT14B	1		C	125	PT34B	1		C
126	PT14A	1		T	126	PT34A	1		T
127	NC	1			127	NC	1		
128	VCC	-			128	VCC	-		
129	PT12B	1	PCLKC1_0	C	129	PT30B	1	PCLKC1_0	C
130	PT12A	1	PCLKT1_0	T	130	PT30A	1	PCLKT1_0	T
131	PT10B	0	PCLKC0_0	C	131	PT28B	0	PCLKC0_0	C
132	XRES	0			132	XRES	0		

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/6-SE					LFE2-12E/12SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
133	GND	-			133	GND	-		
134	PT10A	0	PCLKT0_0	T	134	PT28A	0	PCLKT0_0	T
135	VCC	-			135	VCC	-		
136	PT6B	0		C	136	PT16B	0		C
137	PT6A	0		T	137	PT16A	0		T
138	GND	-			138	GND	-		
139	VCCIO0	0			139	VCCIO0	0		
140	PT4B	0		C	140	PT6B	0		C
141	PT4A	0		T	141	PT6A	0		T
142	VCCAUX	-			142	VCCAUX	-		
143	PT2B	0	VREF2_0	C	143	PT2B	0	VREF2_0	C
144	PT2A	0	VREF1_0	T	144	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 208 PQFP

LFE2-12E/12SE					LFE2-20E/20SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
1	PL2A	7	VREF2_7	T (LVDS)*	1	PL2A	7	VREF2_7	T (LVDS)*
2	PL2B	7	VREF1_7	C (LVDS)*	2	PL2B	7	VREF1_7	C (LVDS)*
3	PL4A	7		T (LVDS)*	3	PL6A	7		T (LVDS)*
4	PL4B	7		C (LVDS)*	4	PL6B	7		C (LVDS)*
5	GND	-			5	GND	-		
6	PL6A	7		T (LVDS)*	6	PL12A	7		T (LVDS)*
7	VCCAUX	-			7	VCCAUX	-		
8	PL6B	7		C (LVDS)*	8	PL12B	7		C (LVDS)*
9	PL8A	7		T (LVDS)*	9	PL14A	7		T (LVDS)*
10	VCCIO7	7			10	VCCIO7	7		
11	PL8B	7		C (LVDS)*	11	PL14B	7		C (LVDS)*
12	VCC	-			12	VCC	-		
13	GND	-			13	GND	-		
14	VCCIO7	7			14	VCCIO7	7		
15	PL12A	7		T (LVDS)*	15	PL18A	7		T (LVDS)*
16	PL12B	7		C (LVDS)*	16	PL18B	7		C (LVDS)*
17	GND	-			17	GND	-		
18	PL13A	7	PCLKT7_0	T	18	PL19A	7	PCLKT7_0	T
19	VCC	-			19	VCC	-		
20	PL13B	7	PCLKC7_0	C	20	PL19B	7	PCLKC7_0	C
21	PL15A	6	PCLKT6_0	T (LVDS)*	21	PL21A	6	PCLKT6_0	T (LVDS)*
22	PL15B	6	PCLKC6_0	C (LVDS)*	22	PL21B	6	PCLKC6_0	C (LVDS)*
23	PL16A	6	VREF2_6	T	23	PL22A	6	VREF2_6	T
24	PL16B	6	VREF1_6	C	24	PL22B	6	VREF1_6	C
25	GND	-			25	GND	-		
26	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	26	PL27A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
27	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	27	PL27B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
28	VCC	-			28	VCC	-		
29	LLM0_PLLCAP	6			29	LLM0_PLLCAP	6		
30	VCCAUX	-			30	VCCAUX	-		
31	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	31	PL30A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
32	GND	-			32	GND	-		
33	PL21A	6	LLM0_GPLLT_FB_A	T	33	PL31A	6	LLM0_GPLLT_FB_A	T
34	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	34	PL30B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
35	PL21B	6	LLM0_GPLLC_FB_A	C	35	PL31B	6	LLM0_GPLLC_FB_A	C
36	PL23A	6			36	PL33A	6		
37	PL24A	6		T (LVDS)*	37	PL38A	6		T (LVDS)*
38	VCCIO6	6			38	VCCIO6	6		
39	PL24B	6		C (LVDS)*	39	PL38B	6		C (LVDS)*
40	VCC	-			40	VCC	-		
41	PL26A	6		T (LVDS)*	41	PL40A	6		T (LVDS)*
42	GND	-			42	GND	-		
43	PL26B	6		C (LVDS)*	43	PL40B	6		C (LVDS)*
44	VCCIO6	6			44	VCCIO6	6		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
45	PL28A	6	LDQS28	T (LVDS)*	45	PL42A	6	LDQS42	T (LVDS)*
46	PL28B	6		C (LVDS)*	46	PL42B	6		C (LVDS)*
47	PL30A	6			47	PL44A	6		
48	TCK	-			48	TCK	-		
49	TDI	-			49	TDI	-		
50	TDO	-			50	TDO	-		
51	VCCJ	-			51	VCCJ	-		
52	TMS	-			52	TMS	-		
53	PB2A	5	VREF2_5	T	53	PB2A	5	VREF2_5	T
54	PB2B	5	VREF1_5	C	54	PB2B	5	VREF1_5	C
55	VCCIO5	5			55	VCCIO5	5		
56	PB6A	5	BDQS6	T	56	PB6A	5	BDQS6	T
57	PB6B	5		C	57	PB6B	5		C
58	PB8A	5		T	58	PB8A	5		T
59	PB8B	5		C	59	PB8B	5		C
60	GND	-			60	GND	-		
61	PB12A	5		T	61	PB12A	5		T
62	PB12B	5		C	62	PB12B	5		C
63	VCCIO5	5			63	VCCIO5	5		
64	PB16A	5		T	64	PB16A	5		T
65	PB16B	5		C	65	PB16B	5		C
66	PB18A	5		T	66	PB18A	5		T
67	PB18B	5		C	67	PB18B	5		C
68	GND	-			68	GND	-		
69	PB20A	5		T	69	PB30A	5		T
70	VCCAUX	-			70	VCCAUX	-		
71	PB20B	5		C	71	PB30B	5		C
72	PB22A	5		T	72	PB32A	5		T
73	PB22B	5		C	73	PB32B	5		C
74	VCC	-			74	VCC	-		
75	PB26A	5	PCLKT5_0	T	75	PB35A	5	PCLKT5_0	T
76	PB26B	5	PCLKC5_0	C	76	PB35B	5	PCLKC5_0	C
77	GND	-			77	GND	-		
78	PB31A	4	PCLKT4_0	T	78	PB40A	4	PCLKT4_0	T
79	PB31B	4	PCLKC4_0	C	79	PB40B	4	PCLKC4_0	C
80	VCC	-			80	VCC	-		
81	GND	-			81	GND	-		
82	PB34A	4		T	82	PB42A	4	BDQS42	T
83	PB34B	4		C	83	PB42B	4		C
84	PB36A	4		T	84	PB44A	4		T
85	PB36B	4		C	85	PB44B	4		C
86	VCCAUX	-			86	VCCAUX	-		
87	PB40A	4		T	87	PB50A	4		T
88	PB40B	4		C	88	PB50B	4		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
89	GND	-			89	GND	-		
90	PB42A	4	BDQS42	T	90	PB52A	4		T
91	PB42B	4		C	91	PB52B	4		C
92	PB44A	4		T	92	PB54A	4		T
93	VCCIO4	4			93	VCCIO4	4		
94	PB44B	4		C	94	PB54B	4		C
95	PB48A	4		T	95	PB58A	4		T
96	PB48B	4		C	96	PB58B	4		C
97	VCC	-			97	VCC	-		
98	PB52A	4		T	98	PB60A	4	BDQS60	T
99	PB52B	4		C	99	PB60B	4		C
100	VCCIO4	4			100	VCCIO4	4		
101	PB54A	4			101	PB63A	4		
102	GND	-			102	GND	-		
103	PB55A	4	VREF2_4	T	103	PB64A	4	VREF2_4	T
104	PB55B	4	VREF1_4	C	104	PB64B	4	VREF1_4	C
105	CFG1	8			105	CFG1	8		
106	PROGRAMN	8			106	PROGRAMN	8		
107	CFG2	8			107	CFG2	8		
108	INITN	8			108	INITN	8		
109	CFG0	8			109	CFG0	8		
110	CCLK	8			110	CCLK	8		
111	DONE	8			111	DONE	8		
112	PR29A	8	D0		112	PR43A	8	D0	
113	VCCIO8	8			113	VCCIO8	8		
114	PR26A	8	D6		114	PR40A	8	D6	
115	GND	-			115	GND	-		
116	VCC	-			116	VCC	-		
117	PR25B	8	D7	C	117	PR39B	8	D7	C
118	VCCIO8	8			118	VCCIO8	8		
119	PR25A	8	DI/CSSPI0N	T	119	PR39A	8	DI/CSSPI0N	T
120	PR24B	8	DOUT/CSON	C	120	PR38B	8	DOUT/CSON	C
121	PR24A	8	BUSY/SISPI	T	121	PR38A	8	BUSY/SISPI	T
122	GND	-			122	GND	-		
123	VCCIO3	3			123	VCCIO3	3		
124	PR21A	3	RLM0_GPLLT_FB_A		124	PR31A	3	RLM0_GPLLT_FB_A	
125	VCCAUX	-			125	VCCAUX	-		
126	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	126	PR30B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
127	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	127	PR30A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
128	RLM0_PLLCAP	3			128	RLM0_PLLCAP	3		
129	VCC	-			129	VCC	-		
130	PR18B	3	RLM0_GDLLC_FB_A	C	130	PR28B	3	RLM0_GDLLC_FB_A	C
131	PR18A	3	RLM0_GDLLT_FB_A	T	131	PR28A	3	RLM0_GDLLT_FB_A**	T
132	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	132	PR27B	3	RLM0_GDLLC_IN_A	C (LVDS)*

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
133	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	133	PR27A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
134	PR16B	3	VREF2_3	C	134	PR22B	3	VREF2_3	C
135	VCCIO3	3			135	VCCIO3	3		
136	PR16A	3	VREF1_3	T	136	PR22A	3	VREF1_3	T
137	PR15B	3	PCLKC3_0	C (LVDS)*	137	PR21B	3	PCLKC3_0	C (LVDS)*
138	PR15A	3	PCLKT3_0	T (LVDS)*	138	PR21A	3	PCLKT3_0	T (LVDS)*
139	GND	-			139	GND	-		
140	VCC	-			140	VCC	-		
141	PR13B	2	PCLKC2_0	C	141	PR19B	2	PCLKC2_0	C
142	PR13A	2	PCLKT2_0	T	142	PR19A	2	PCLKT2_0	T
143	VCCIO2	2			143	VCCIO2	2		
144	PR12A	2			144	PR16A	2	RDQS16	
145	GND	-			145	GND	-		
146	VCC	-			146	VCC	-		
147	PR8B	2		C (LVDS)*	147	PR14B	2		C (LVDS)*
148	VCCIO2	2			148	VCCIO2	2		
149	PR8A	2		T (LVDS)*	149	PR14A	2		T (LVDS)*
150	PR6B	2		C (LVDS)*	150	PR12B	2		C (LVDS)*
151	VCCAUX	-			151	VCCAUX	-		
152	PR6A	2		T (LVDS)*	152	PR12A	2		T (LVDS)*
153	PR4B	2		C (LVDS)*	153	PR6B	2		C (LVDS)*
154	PR4A	2		T (LVDS)*	154	PR6A	2		T (LVDS)*
155	PR2B	2	VREF2_2	C (LVDS)*	155	PR2B	2	VREF2_2	C (LVDS)*
156	PR2A	2	VREF1_2	T (LVDS)*	156	PR2A	2	VREF1_2	T (LVDS)*
157	PT55B	1	VREF2_1	C	157	PT64B	1	VREF2_1	C
158	PT55A	1	VREF1_1	T	158	PT64A	1	VREF1_1	T
159	GND	-			159	GND	-		
160	PT54B	1		C	160	PT62B	1		C
161	PT54A	1		T	161	PT62A	1		T
162	VCCIO1	1			162	VCCIO1	1		
163	PT52B	1		C	163	PT60B	1		C
164	PT52A	1		T	164	PT60A	1		T
165	PT50B	1		C	165	PT58B	1		C
166	PT50A	1		T	166	PT58A	1		T
167	PT48B	1		C	167	PT56B	1		C
168	PT48A	1		T	168	PT56A	1		T
169	GND	-			169	GND	-		
170	VCCIO1	1			170	VCCIO1	1		
171	VCC	-			171	VCC	-		
172	PT40B	1		C	172	PT50B	1		C
173	PT40A	1		T	173	PT50A	1		T
174	VCCAUX	-			174	VCCAUX	-		
175	GND	-			175	GND	-		
176	PT36B	1		C	176	PT44B	1		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Pin Number	Pin Function	Bank	Dual Function	Differential	Pin Number	Pin Function	Bank	Dual Function	Differential
177	PT36A	1		T	177	PT44A	1		T
178	PT34B	1		C	178	PT42B	1		C
179	PT34A	1		T	179	PT42A	1		T
180	PT30B	1	PCLKC1_0	C	180	PT39B	1	PCLKC1_0	C
181	PT30A	1	PCLKT1_0	T	181	PT39A	1	PCLKT1_0	T
182	XRES	1			182	XRES	1		
183	PT28B	0	PCLKC0_0	C	183	PT37B	0	PCLKC0_0	C
184	GND	-			184	GND	-		
185	PT28A	0	PCLKT0_0	T	185	PT37A	0	PCLKT0_0	T
186	PT26B	0		C	186	PT36B	0		C
187	PT26A	0		T	187	PT36A	0		T
188	VCC	-			188	VCC	-		
189	PT20B	0		C	189	PT30B	0		C
190	VCCAUX	-			190	VCCAUX	-		
191	PT20A	0		T	191	PT30A	0		T
192	GND	-			192	GND	-		
193	PT18B	0		C	193	PT26B	0		C
194	PT18A	0		T	194	PT26A	0		T
195	VCCIO0	0			195	VCCIO0	0		
196	PT16B	0		C	196	PT20B	0		C
197	PT16A	0		T	197	PT20A	0		T
198	VCC	-			198	VCC	-		
199	PT12B	0		C	199	PT12B	0		C
200	PT12A	0		T	200	PT12A	0		T
201	GND	-			201	GND	-		
202	PT8B	0		C	202	PT8B	0		C
203	PT8A	0		T	203	PT8A	0		T
204	PT6B	0		C	204	PT6B	0		C
205	PT6A	0		T	205	PT6A	0		T
206	VCCIO0	0			206	VCCIO0	0		
207	PT2B	0	VREF2_0	C	207	PT2B	0	VREF2_0	C
208	PT2A	0	VREF1_0	T	208	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
C3	PL2A	7	VREF2_7	T (LVDS)*	C3	PL2A	7	VREF2_7	T (LVDS)*
C2	PL2B	7	VREF1_7	C (LVDS)*	C2	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
-	-	-			-	-	-		
D3	PL5A	7		T	D3	PL5A	7		T
D4	PL4A	7		T (LVDS)*	D4	PL4A	7		T (LVDS)*
D2	PL5B	7		C	D2	PL5B	7		C
GND	GNDIO7	7			GNDIO	GNDIO7	7		
E4	PL4B	7		C (LVDS)*	E4	PL4B	7		C (LVDS)*
B1	PL7A	7		T	B1	PL7A	7		T
C1	PL7B	7		C	C1	PL7B	7		C
F5	PL9A	7		T	F5	PL9A	7		T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
F4	PL8A	7		T (LVDS)*	F4	PL8A	7		T (LVDS)*
G6	PL9B	7		C	G6	PL9B	7		C
G4	PL8B	7		C (LVDS)*	G4	PL8B	7		C (LVDS)*
D1	PL10A	7	LDQS10	T (LVDS)*	D1	PL10A	7	LDQS10	T (LVDS)*
GND	GNDIO7	7			GND	GNDIO7	7		
E1	PL10B	7		C (LVDS)*	E1	PL10B	7		C (LVDS)*
F3	PL11A	7		T	F3	PL11A	7		T
G3	PL11B	7		C	G3	PL11B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
F2	PL12A	7		T (LVDS)*	F2	PL12A	7		T (LVDS)*
F1	PL12B	7		C (LVDS)*	F1	PL12B	7		C (LVDS)*
GND	GNDIO7	7			GND	GNDIO7	7		
G2	PL13A	7	PCLKT7_0	T	G2	PL13A	7	PCLKT7_0	T
G1	PL13B	7	PCLKC7_0	C	G1	PL13B	7	PCLKC7_0	C
H6	PL15A	6	PCLKT6_0	T (LVDS)*	H6	PL15A	6	PCLKT6_0	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
H5	PL15B	6	PCLKC6_0	C (LVDS)*	H5	PL15B	6	PCLKC6_0	C (LVDS)*
H4	PL16A	6	VREF2_6	T	H4	PL16A	6	VREF2_6	T
GND	GNDIO6	6			GND	GNDIO6	6		
H3	PL16B	6	VREF1_6	C	H3	PL16B	6	VREF1_6	C
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
G10	VCC	-			G10	VCC	-		
J4	PL18A	6	LLM0_GDLLT_FB_A	T	J4	PL18A	6	LLM0_GDLLT_FB_A	T
J5	PL18B	6	LLM0_GDLLC_FB_A	C	J5	PL18B	6	LLM0_GDLLC_FB_A	C
J6	LLM0_PLLCAP	6			J6	LLM0_PLLCAP	6		
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
GND	GNDIO6	6			GND	GNDIO6	6		
J1	PL21A	6	LLM0_GPLLT_FB_A	T	J1	PL21A	6	LLM0_GPLLT_FB_A	T
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J2	PL21B	6	LLM0_GPLLC_FB_A	C	J2	PL21B	6	LLM0_GPLLC_FB_A	C
GND	GNDIO6	6			GND	GNDIO6	6		
L2	PL24A	6		T (LVDS)*	L2	PL24A	6		T (LVDS)*
K2	PL25A	6		T	K2	PL25A	6		T
L3	PL24B	6		C (LVDS)*	L3	PL24B	6		C (LVDS)*
K1	PL25B	6		C	K1	PL25B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
L4	PL26A	6		T (LVDS)*	L4	PL26A	6		T (LVDS)*
L1	PL27A	6		T	L1	PL27A	6		T
L5	PL26B	6		C (LVDS)*	L5	PL26B	6		C (LVDS)*
M1	PL27B	6		C	M1	PL27B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
N1	PL29A	6		T	N1	PL29A	6		T
N2	PL28A	6	LDQS28	T (LVDS)*	N2	PL28A	6	LDQS28	T (LVDS)*
P1	PL29B	6		C	P1	PL29B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
P2	PL28B	6		C (LVDS)*	P2	PL28B	6		C (LVDS)*
R1	PL30A	6		T (LVDS)*	R1	PL30A	6		T (LVDS)*
GND	GNDIO6	6			GND	GNDIO6	6		
R2	PL30B	6		C (LVDS)*	R2	PL30B	6		C (LVDS)*
N4	TDI	-			N4	TDI	-		
M4	TCK	-			M4	TCK	-		
P3	TDO	-			P3	TDO	-		
N3	TMS	-			N3	TMS	-		
K7	VCCJ	-			K7	VCCJ	-		
M5	PB2A	5	VREF2_5	T	M5	PB2A	5	VREF2_5	T
K6	NC	-			K6	PB3A	5		
M6	PB2B	5	VREF1_5	C	M6	PB2B	5	VREF1_5	C
R3	NC	-			R3	PB5A	5		T
P4	NC	-			P4	PB5B	5		C
-	-	-			VCC	VCCIO	5		
-	-	-			GND	GNDIO5	5		
N5	PB3A	5		T	N5	PB21A	5		T
N6	PB3B	5		C	N6	PB21B	5		C
T2	PB4A	5		T	T2	PB22A	5		T
P6	PB5A	5		T	P6	PB23A	5		T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
T3	PB4B	5		C	T3	PB22B	5		C
R6	PB5B	5		C	R6	PB23B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
R4	PB6A	5	BDQS6	T	R4	PB24A	5	BDQS24	T
L6	PB7A	5		T	L6	PB25A	5		T
T4	PB6B	5		C	T4	PB24B	5		C
L7	PB7B	5		C	L7	PB25B	5		C

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
N7	PB8A	5	PCLKT5_0	T	N7	PB26A	5	PCLKT5_0	T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
M8	PB8B	5	PCLKC5_0	C	M8	PB26B	5	PCLKC5_0	C
GND	GNDIO5	5			GND	GNDIO5	5		
P7	PB13A	4	PCLKT4_0	T	P7	PB31A	4	PCLKT4_0	T
R8	PB13B	4	PCLKC4_0	C	R8	PB31B	4	PCLKC4_0	C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
T5	PB14A	4		T	T5	PB32A	4		T
T6	PB14B	4		C	T6	PB32B	4		C
T8	PB15A	4	BDQS15	T	T8	PB33A	4	BDQS33	T
GND	GNDIO4	4			GND	GNDIO4	4		
R7	PB16A	4		T	R7	PB34A	4		T
T9	PB15B	4		C	T9	PB33B	4		C
T7	PB16B	4		C	T7	PB34B	4		C
L8	PB17A	4		T	L8	PB35A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
P8	PB18A	4		T	P8	PB36A	4		T
L9	PB17B	4		C	L9	PB35B	4		C
N8	PB18B	4		C	N8	PB36B	4		C
R9	PB19A	4		T	R9	PB37A	4		T
GND	GNDIO4	4			GND	GNDIO4	4		
R10	PB19B	4		C	R10	PB37B	4		C
-	-	-			VCC	VCCIO	4		
-	-	-			GND	GNDIO4	4		
N9	PB20A	4		T	N9	PB47A	4		T
T10	PB21A	4		T	T10	PB48A	4		T
M9	PB20B	4		C	M9	PB47B	4		C
R11	PB21B	4		C	R11	PB48B	4		C
P10	PB22A	4		T	P10	PB49A	4		T
N11	PB23A	4		T	N11	PB50A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
N10	PB22B	4		C	N10	PB49B	4		C
P11	PB23B	4		C	P11	PB50B	4		C
T11	PB24A	4	BDQS24	T	T11	PB51A	4	BDQS51	T
GND	GNDIO4	4			GND	GNDIO4	4		
M11	PB25A	4		T	M11	PB52A	4		T
T12	PB24B	4		C	T12	PB51B	4		C
L11	PB25B	4		C	L11	PB52B	4		C
T13	PB26A	4		T	T13	PB53A	4		T
R13	PB27A	4		T	R13	PB54A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
T14	PB26B	4		C	T14	PB53B	4		C
P13	PB27B	4		C	P13	PB54B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
N12	PB28A	4	VREF2_4	T	N12	PB55A	4	VREF2_4	T
M12	PB28B	4	VREF1_4	C	M12	PB55B	4	VREF1_4	C
R15	CFG2	8			R15	CFG2	8		
N14	CFG1	8			N14	CFG1	8		
N13	PROGRAMN	8			N13	PROGRAMN	8		
N15	CFG0	8			N15	CFG0	8		
P15	PR30B	8	WRITEN	C	P15	PR30B	8	WRITEN	C
L12	INITN	8			L12	INITN	8		
N16	PR29B	8	CSN	C	N16	PR29B	8	CSN	C
GND	GNDIO8	8			GND	GNDIO8	8		
R14	CCLK	8			R14	CCLK	8		
P14	PR30A	8	CS1N	T	P14	PR30A	8	CS1N	T
M13	DONE	8			M13	DONE	8		
R16	PR28B	8	D1	C	R16	PR28B	8	D1	C
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		
M16	PR29A	8	D0	T	M16	PR29A	8	D0	T
P16	PR28A	8	D2	T	P16	PR28A	8	D2	T
L15	PR27B	8	D3	C	L15	PR27B	8	D3	C
GND	GNDIO8	8			GND	GNDIO8	8		
L14	PR26A	8	D6	T	L14	PR26A	8	D6	T
L16	PR27A	8	D4	T	L16	PR27A	8	D4	T
L10	PR25B	8	D7	C	L10	PR25B	8	D7	C
L13	PR26B	8	D5	C	L13	PR26B	8	D5	C
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		
K11	PR25A	8	DI/CSSPI0N	T	K11	PR25A	8	DI/CSSPI0N	T
K14	PR24B	8	DOUT/CSON	C	K14	PR24B	8	DOUT/CSON	C
K13	PR24A	8	BUSY/SISPI	T	K13	PR24A	8	BUSY/SISPI	T
GND	GNDIO8	8			GND	GNDIO8	8		
K15	PR21B	3	RLM0_GPLLC_FB_A	C	K15	PR21B	3	RLM0_GPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
K16	PR21A	3	RLM0_GPLLT_FB_A	T	K16	PR21A	3	RLM0_GPLLT_FB_A	T
GND	GNDIO3	3			GND	GNDIO3	3		
J16	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	J16	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
J15	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	J15	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
J14	RLM0_PLLCAP	3			J14	RLM0_PLLCAP	3		
J13	PR18B	3	RLM0_GDLLC_FB_A	C	J13	PR18B	3	RLM0_GDLLC_FB_A	C
J12	PR18A	3	RLM0_GDLLT_FB_A	T	J12	PR18A	3	RLM0_GDLLT_FB_A	T
H12	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	H12	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
GND	GNDIO3	3			GND	GNDIO3	3		
H13	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	H13	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
H15	PR16B	3	VREF2_3	C	H15	PR16B	3	VREF2_3	C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
H16	PR16A	3	VREF1_3	T	H16	PR16A	3	VREF1_3	T
H11	PR15B	3	PCLKC3_0	C (LVDS)*	H11	PR15B	3	PCLKC3_0	C (LVDS)*

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J11	PR15A	3	PCLKT3_0	T (LVDS)*	J11	PR15A	3	PCLKT3_0	T (LVDS)*
G16	PR13B	2	PCLKC2_0	C	G16	PR13B	2	PCLKC2_0	C
GND	GNDIO2	2			GND	GNDIO2	2		
G15	PR13A	2	PCLKT2_0	T	G15	PR13A	2	PCLKT2_0	T
F15	PR11B	2		C	F15	PR11B	2		C
G11	PR12B	2		C (LVDS)*	G11	PR12B	2		C (LVDS)*
F14	PR11A	2		T	F14	PR11A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
F12	PR12A	2		T (LVDS)*	F12	PR12A	2		T (LVDS)*
G14	PR10B	2		C (LVDS)*	G14	PR10B	2		C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	G13	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	2			GND	GNDIO2	2		
F16	PR8B	2		C (LVDS)*	F16	PR8B	2		C (LVDS)*
F9	PR9B	2		C	F9	PR9B	2		C
E16	PR8A	2		T (LVDS)*	E16	PR8A	2		T (LVDS)*
F10	PR9A	2		T	F10	PR9A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
D16	PR7B	2		C	D16	PR7B	2		C
D15	PR7A	2		T	D15	PR7A	2		T
C15	PR4B	2		C (LVDS)*	C15	PR4B	2		C (LVDS)*
C16	PR5B	2		C	C16	PR5B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
D14	PR4A	2		T (LVDS)*	D14	PR4A	2		T (LVDS)*
B16	PR5A	2		T	B16	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	F13	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	E13	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	F11	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	E11	PT55A	1	VREF1_1	T
GND	GNDIO1	1			GND	GNDIO1	1		
A15	PT27B	1		C	A15	PT54B	1		C
E12	PT26B	1		C	E12	PT53B	1		C
B15	PT27A	1		T	B15	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
D12	PT26A	1		T	D12	PT53A	1		T
B14	PT25B	1		C	B14	PT52B	1		C
C14	PT24B	1		C	C14	PT51B	1		C
A14	PT25A	1		T	A14	PT52A	1		T
D13	PT24A	1		T	D13	PT51A	1		T
C13	PT23B	1		C	C13	PT50B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
A13	PT22B	1		C	A13	PT49B	1		C
B13	PT23A	1		T	B13	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A12	PT22A	1		T	A12	PT49A	1		T
B11	PT21B	1		C	B11	PT48B	1		C
D11	PT20B	1		C	D11	PT47B	1		C
A11	PT21A	1		T	A11	PT48A	1		T
C11	PT20A	1		T	C11	PT47A	1		T
-	-	-			GND	GNDIO1	1		
-	-	-			VCC	VCCIO	1		
D10	PT19B	1		C	D10	PT37B	1		C
C10	PT19A	1		T	C10	PT37A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
B10	PT18B	1		C	B10	PT36B	1		C
A9	PT17B	1		C	A9	PT35B	1		C
A10	PT18A	1		T	A10	PT36A	1		T
B9	PT17A	1		T	B9	PT35A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
A8	PT16B	1		C	A8	PT34B	1		C
D9	PT15B	1		C	D9	PT33B	1		C
B8	PT16A	1		T	B8	PT34A	1		T
C9	PT15A	1		T	C9	PT33A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
B7	PT14B	1		C	B7	PT32B	1		C
E9	PT13B	1		C	E9	PT31B	1		C
A7	PT14A	1		T	A7	PT32A	1		T
D8	PT13A	1		T	D8	PT31A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
A6	PT12B	1	PCLKC1_0	C	A6	PT30B	1	PCLKC1_0	C
B6	PT12A	1	PCLKT1_0	T	B6	PT30A	1	PCLKT1_0	T
E6	XRES	-			E6	XRES	1		
F8	PT10B	0	PCLKC0_0	C	F8	PT28B	0	PCLKC0_0	C
GND	GNDIO0	0			GND	GNDIO0	0		
E8	PT10A	0	PCLKT0_0	T	E8	PT28A	0	PCLKT0_0	T
A5	PT9B	0		C	A5	PT27B	0		C
A3	PT8B	0		C	A3	PT26B	0		C
A4	PT9A	0		T	A4	PT27A	0		T
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
B3	PT8A	0		T	B3	PT26A	0		T
A2	PT7B	0		C	A2	PT25B	0		C
C7	PT6B	0		C	C7	PT24B	0		C
B2	PT7A	0		T	B2	PT25A	0		T
D7	PT6A	0		T	D7	PT24A	0		T
D6	PT5B	0		C	D6	PT23B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
F7	PT4B	0		C	F7	PT22B	0		C
C6	PT5A	0		T	C6	PT23A	0		T

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
F6	PT4A	0		T	F6	PT22A	0		T
C4	PT3B	0		C	C4	PT21B	0		C
B4	PT3A	0		T	B4	PT21A	0		T
-	-	-			GND	GNDIO0	0		
-	-	-			VCC	VCCIO	0		
D5	PT2B	0	VREF2_0	C	D5	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	E5	PT2A	0	VREF1_0	T
G7	VCC	-			G7	VCC	-		
G9	VCC	-			G9	VCC	-		
H7	VCC	-			H7	VCC	-		
J10	VCC	-			J10	VCC	-		
K10	VCC	-			K10	VCC	-		
K8	VCC	-			K8	VCC	-		
G8	VCCAUX	-			G8	VCCAUX	-		
H10	VCCAUX	-			H10	VCCAUX	-		
J7	VCCAUX	-			J7	VCCAUX	-		
K9	VCCAUX	-			K9	VCCAUX	-		
C5	VCCIO	0			C5	VCCIO	0		
E7	VCCIO	0			E7	VCCIO	0		
C12	VCCIO	1			C12	VCCIO	1		
E10	VCCIO	1			E10	VCCIO	1		
E14	VCCIO	2			E14	VCCIO	2		
G12	VCCIO	2			G12	VCCIO	2		
K12	VCCIO	3			K12	VCCIO	3		
M14	VCCIO	3			M14	VCCIO	3		
M10	VCCIO	4			M10	VCCIO	4		
P12	VCCIO	4			P12	VCCIO	4		
M7	VCCIO	5			M7	VCCIO	5		
P5	VCCIO	5			P5	VCCIO	5		
K5	VCCIO	6			K5	VCCIO	6		
M3	VCCIO	6			M3	VCCIO	6		
E3	VCCIO	7			E3	VCCIO	7		
G5	VCCIO	7			G5	VCCIO	7		
T15	VCCIO	8			T15	VCCIO	8		
A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-		
B12	GND	-			B12	GND	-		
B5	GND	-			B5	GND	-		
C8	GND	-			C8	GND	-		
E15	GND	-			E15	GND	-		
E2	GND	-			E2	GND	-		
H14	GND	-			H14	GND	-		
H8	GND	-			H8	GND	-		

LFE2-6E/6SE and LFE2-12E/12SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/6SE					LFE2-12E/12SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
H9	GND	-			H9	GND	-		
J3	GND	-			J3	GND	-		
J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-		
M15	GND	-			M15	GND	-		
M2	GND	-			M2	GND	-		
P9	GND	-			P9	GND	-		
R12	GND	-			R12	GND	-		
R5	GND	-			R5	GND	-		
T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA

Ball Number	Ball Function	Bank	Dual Function	Differential
C3	PL2A	7	VREF2_7	T*
C2	PL2B	7	VREF1_7	C*
VCCIO	VCCIO7	7		
GND	GNDIO	7		
D3	PL7A	7		T
D4	PL6A	7		T*
D2	PL7B	7		C
GND	GNDIO	7		
E4	PL6B	7		C*
B1	PL13A	7		T
C1	PL13B	7		C
F5	PL15A	7		T
F4	PL14A	7		T*
G6	PL15B	7		C
G4	PL14B	7		C*
D1	PL16A	7	LDQS16	T*
GND	GNDIO	7		
VCC	VCCIO	7		
E1	PL16B	7		C*
F3	PL17A	7		T
G3	PL17B	7		C
VCCIO	VCCIO7	7		
F2	PL18A	7		T*
F1	PL18B	7		C*
GND	GNDIO	7		
G2	PL19A	7	PCLKT7_0	T
G1	PL19B	7	PCLKC7_0	C
H6	PL21A	6	PCLKT6_0	T*
VCCIO	VCCIO6	6		
H5	PL21B	6	PCLKC6_0	C*
H4	PL22A	6	VREF2_6	T
GND	GNDIO	6		
H3	PL22B	6	VREF1_6	C
H2	PL27A	6	LLM0_GDLLT_IN_A**	T*
H1	PL27B	6	LLM0_GDLLC_IN_A**	C*
G10	VCC	-		
J4	PL28A	6	LLM0_GDLLT_FB_A	T
J5	PL28B	6	LLM0_GDLLC_FB_A	C
J6	LLM0_PLLCAP	6		
K4	PL30A	6	LLM0_GPLLT_IN_A**	T*
GND	GNDIO	6		
J1	PL31A	6	LLM0_GPLLT_FB_A	T
K3	PL30B	6	LLM0_GPLLC_IN_A**	C*

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO6	6		
J2	PL31B	6	LLM0_GPLLC_FB_A	C
GND	GNDIO	6		
L2	PL38A	6		T*
K2	PL39A	6		T
L3	PL38B	6		C*
K1	PL39B	6		C
VCCIO	VCCIO6	6		
L4	PL40A	6		T*
L1	PL41A	6		T
L5	PL40B	6		C*
M1	PL41B	6		C
GND	GNDIO	6		
N1	PL43A	6		T
N2	PL42A	6	LDQS42	T*
P1	PL43B	6		C
VCCIO	VCCIO6	6		
P2	PL42B	6		C*
R1	PL44A	6		T*
GND	GNDIO	6		
R2	PL44B	6		C*
N4	TDI	-		
M4	TCK	-		
P3	TDO	-		
N3	TMS	-		
K7	VCCJ	-		
M5	PB2A	5	VREF2_5	T
K6	PB3A	5		
M6	PB2B	5	VREF1_5	C
R3	PB5A	5		T
P4	PB5B	5		C
VCC	VCCIO	5		
GND	GNDIO	5		
N5	PB30A	5		T
N6	PB30B	5		C
T2	PB31A	5		T
P6	PB32A	5		T
VCCIO	VCCIO5	5		
T3	PB31B	5		C
R6	PB32B	5		C
GND	GNDIO	5		
R4	PB33A	5	BDQS33	T
L6	PB34A	5		T
T4	PB33B	5		C

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
L7	PB34B	5		C
N7	PB35A	5	PCLKT5_0	T
VCCIO	VCCIO5	5		
M8	PB35B	5	PCLKC5_0	C
GND	GNDIO	5		
P7	PB40A	4	PCLKT4_0	T
R8	PB40B	4	PCLKC4_0	C
VCCIO	VCCIO4	4		
T5	PB41A	4		T
T6	PB41B	4		C
T8	PB42A	4	BDQS42	T
GND	GNDIO	4		
R7	PB43A	4		T
T9	PB42B	4		C
T7	PB43B	4		C
L8	PB44A	4		T
VCCIO	VCCIO4	4		
P8	PB45A	4		T
L9	PB44B	4		C
N8	PB45B	4		C
R9	PB46A	4		T
GND	GNDIO	4		
R10	PB46B	4		C
VCC	VCCIO	4		
GND	GNDIO	4		
N9	PB56A	4		T
T10	PB57A	4		T
M9	PB56B	4		C
R11	PB57B	4		C
P10	PB58A	4		T
N11	PB59A	4		T
VCCIO	VCCIO4	4		
N10	PB58B	4		C
P11	PB59B	4		C
T11	PB60A	4	BDQS60	T
GND	GNDIO	4		
M11	PB61A	4		T
T12	PB60B	4		C
L11	PB61B	4		C
T13	PB62A	4		T
R13	PB63A	4		T
VCCIO	VCCIO4	4		
T14	PB62B	4		C
P13	PB63B	4		C

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	4		
N12	PB64A	4	VREF2_4	T
M12	PB64B	4	VREF1_4	C
R15	CFG2	8		
N14	CFG1	8		
N13	PROGRAMN	8		
N15	CFG0	8		
P15	PR44B	8	WRITEN	C
L12	INITN	8		
N16	PR43B	8	CSN	C
GND	GNDIO	8		
R14	CCLK	8		
P14	PR44A	8	CS1N	T
M13	DONE	8		
R16	PR42B	8	D1	C
VCCIO	VCCIO8	8		
M16	PR43A	8	D0	T
P16	PR42A	8	D2	T
L15	PR41B	8	D3	C
GND	GNDIO	8		
L14	PR40A	8	D6	T
L16	PR41A	8	D4	T
L10	PR39B	8	D7	C
L13	PR40B	8	D5	C
VCCIO	VCCIO8	8		
K11	PR39A	8	DI	T
K14	PR38B	8	DOUT,CSON	C
K13	PR38A	8	BUSY	T
GND	GNDIO	8		
K15	PR31B	3	RLM0_GPLLC_FB_A	C
VCCIO	VCCIO3	3		
K16	PR31A	3	RLM0_GPLLT_FB_A	T
GND	GNDIO	3		
J16	PR30B	3	RLM0_GPLLC_IN_A**	C*
J15	PR30A	3	RLM0_GPLLT_IN_A**	T*
J14	RLM0_PLLCAP	3		
J13	PR28B	3	RLM0_GDLLC_FB_A	C
J12	PR28A	3	RLM0_GDLLT_FB_A	T
H12	PR27B	3	RLM0_GDLLC_IN_A**	C*
GND	GNDIO	3		
H13	PR27A	3	RLM0_GDLLT_IN_A**	T*
H15	PR22B	3	VREF2_3	C
VCCIO	VCCIO3	3		
H16	PR22A	3	VREF1_3	T

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
H11	PR21B	3	PCLKC3_0	C*
J11	PR21A	3	PCLKT3_0	T*
G16	PR19B	2	PCLKC2_0	C
GND	GNDIO	2		
G15	PR19A	2	PCLKT2_0	T
F15	PR17B	2		C
G11	PR18B	2		C*
F14	PR17A	2		T
VCCIO	VCCIO2	2		
F12	PR18A	2		T*
G14	PR16B	2		C*
G13	PR16A	2	RDQS16	T*
GND	GNDIO	2		
F16	PR14B	2		C*
F9	PR15B	2		C
E16	PR14A	2		T*
F10	PR15A	2		T
VCCIO	VCCIO2	2		
D16	PR13B	2		C
D15	PR13A	2		T
C15	PR6B	2		C*
C16	PR7B	2		C
GND	GNDIO	2		
D14	PR6A	2		T*
B16	PR7A	2		T
F13	PR2B	2	VREF2_2	C*
VCCIO	VCCIO2	2		
E13	PR2A	2	VREF1_2	T*
F11	PT64B	1	VREF2_1	C
E11	PT64A	1	VREF1_1	T
GND	GNDIO	1		
A15	PT63B	1		C
E12	PT62B	1		C
B15	PT63A	1		T
VCCIO	VCCIO1	1		
D12	PT62A	1		T
B14	PT61B	1		C
C14	PT60B	1		C
A14	PT61A	1		T
D13	PT60A	1		T
C13	PT59B	1		C
GND	GNDIO	1		
A13	PT58B	1		C
B13	PT59A	1		T

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO1	1		
A12	PT58A	1		T
B11	PT57B	1		C
D11	PT56B	1		C
A11	PT57A	1		T
C11	PT56A	1		T
GND	GNDIO	1		
VCC	VCCIO	1		
D10	PT46B	1		C
C10	PT46A	1		T
GND	GNDIO	1		
B10	PT45B	1		C
A9	PT44B	1		C
A10	PT45A	1		T
B9	PT44A	1		T
VCCIO	VCCIO1	1		
A8	PT43B	1		C
D9	PT42B	1		C
B8	PT43A	1		T
C9	PT42A	1		T
GND	GNDIO	1		
B7	PT41B	1		C
E9	PT40B	1		C
A7	PT41A	1		T
D8	PT40A	1		T
VCCIO	VCCIO1	1		
A6	PT39B	1	PCLKC1_0	C
B6	PT39A	1	PCLKT1_0	T
E6	XRES	1		
F8	PT37B	0	PCLKC0_0	C
GND	GNDIO	0		
E8	PT37A	0	PCLKT0_0	T
A5	PT36B	0		C
A3	PT35B	0		C
A4	PT36A	0		T
VCCIO	VCCIO0	0		
B3	PT35A	0		T
A2	PT34B	0		C
C7	PT33B	0		C
B2	PT34A	0		T
D7	PT33A	0		T
D6	PT32B	0		C
GND	GNDIO	0		
F7	PT31B	0		C

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
C6	PT32A	0		T
VCCIO	VCCIO0	0		
F6	PT31A	0		T
C4	PT30B	0		C
B4	PT30A	0		T
GND	GNDIO	0		
VCC	VCCIO	0		
D5	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T
G7	VCC	-		
G9	VCC	-		
H7	VCC	-		
J10	VCC	-		
K10	VCC	-		
K8	VCC	-		
G8	VCCAUX	-		
H10	VCCAUX	-		
J7	VCCAUX	-		
K9	VCCAUX	-		
C5	VCCIO	0		
E7	VCCIO	0		
C12	VCCIO	1		
E10	VCCIO	1		
E14	VCCIO	2		
G12	VCCIO	2		
K12	VCCIO	3		
M14	VCCIO	3		
M10	VCCIO	4		
P12	VCCIO	4		
M7	VCCIO	5		
P5	VCCIO	5		
K5	VCCIO	6		
M3	VCCIO	6		
E3	VCCIO	7		
G5	VCCIO	7		
T15	VCCIO	8		
A1	GND	-		
A16	GND	-		
B12	GND	-		
B5	GND	-		
C8	GND	-		
E15	GND	-		
E2	GND	-		
H14	GND	-		

LFE2-20E/20SE Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
H8	GND	-		
H9	GND	-		
J3	GND	-		
J8	GND	-		
J9	GND	-		
M15	GND	-		
M2	GND	-		
P9	GND	-		
R12	GND	-		
R5	GND	-		
T1	GND	-		
T16	GND	-		

* Supports true LVDS outputs.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E4	PL2A	7	VREF2_7	T*	E4	PL2A	7	VREF2_7	T*
E5	PL2B	7	VREF1_7	C*	E5	PL2B	7	VREF1_7	C*
-	-	-			GND	GNDIO	7		
E3	NC	-			E3	PL4A	7		T*
F4	PL3A	7		T	F4	PL5A	7		T
F3	NC	-			F3	PL4B	7		C*
F5	PL3B	7		C	F5	PL5B	7		C
E2	PL4A	7		T*	E2	PL6A	7		T*
G6	PL5A	7		T	G6	PL7A	7		T
E1	PL4B	7		C*	E1	PL6B	7		C*
G7	PL5B	7		C	G7	PL7B	7		C
GND	GNDIO	7			GND	GNDIO	7		
F1	NC	-			F1	PL9A	7		T
H4	NC	-			H4	PL8A	7	LDQS8	T*
F2	NC	-			F2	PL9B	7		C
H5	NC	-			H5	PL8B	7		C*
G1	NC	-			G1	PL11A	7		T
G3	NC	-			G3	PL10A	7		T*
G2	NC	-			G2	PL11B	7		C
-	-	-			GND	GNDIO	7		
G4	NC	-			G4	PL10B	7		C*
J4	PL7A	7		T	J4	PL13A	7		T
H1	PL6A	7			H1	PL12A	7		
J5	PL7B	7		C	J5	PL13B	7		C
L6	PL9A	7		T	L6	PL15A	7		T
J2	PL8A	7		T*	J2	PL14A	7		T*
L5	PL9B	7		C	L5	PL15B	7		C
J1	PL8B	7		C*	J1	PL14B	7		C*
K3	PL10A	7	LDQS10	T*	K3	PL16A	7	LDQS16	T*
GND	GNDIO	7			GND	GNDIO	7		
K6	NC	-			K6	NC	-		
K4	PL10B	7		C*	K4	PL16B	7		C*
K2	PL11A	7		T	K2	PL17A	7		T
K1	PL11B	7		C	K1	PL17B	7		C
L4	PL12A	7		T*	L4	PL18A	7		T*
L3	PL12B	7		C*	L3	PL18B	7		C*
GND	GNDIO	7			GND	GNDIO	7		
L2	PL13A	7	PCLKT7_0	T	L2	PL19A	7	PCLKT7_0	T
L1	PL13B	7	PCLKC7_0	C	L1	PL19B	7	PCLKC7_0	C
M5	PL15A	6	PCLKT6_0	T*	M5	PL21A	6	PCLKT6_0	T*
M6	PL15B	6	PCLKC6_0	C*	M6	PL21B	6	PCLKC6_0	C*
M3	PL16A	6	VREF2_6	T	M3	PL22A	6	VREF2_6	T
M4	PL16B	6	VREF1_6	C	M4	PL22B	6	VREF1_6	C
N1	NC	-			N1	PL24A	6		T

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
M2	NC	-			M2	PL23A	6		T*
N2	NC	-			N2	PL24B	6		C
M1	NC	-			M1	PL23B	6		C*
GND	GNDIO	6			GND	GNDIO	6		
N3	NC	-			N3	PL25A	6	LDQS25	T*
N5	NC	-			N5	PL26A	6		T
N4	NC	-			N4	PL25B	6		C*
P5	NC	-			P5	PL26B	6		C
P1	PL17A	6	LLM0_GDLLT_IN_A**	T*	P1	PL27A	6	LLM0_GDLLT_IN_A**	T*
P2	PL17B	6	LLM0_GDLLC_IN_A**	C*	P2	PL27B	6	LLM0_GDLLC_IN_A**	C*
P4	PL18A	6	LLM0_GDLLT_FB_A	T	P4	PL28A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO	6			GND	GNDIO	6		
R4	PL18B	6	LLM0_GDLLC_FB_A	C	R4	PL28B	6	LLM0_GDLLC_FB_A	C
N6	VCC	-			N6	VCC	-		
P6	LLM0_PLLCAP	6			P6	LLM0_PLLCAP	6		
R1	PL20A	6	LLM0_GPLLT_IN_A**	T*	R1	PL30A	6	LLM0_GPLLT_IN_A**	T*
R3	PL21A	6	LLM0_GPLLT_FB_A	T	R3	PL31A	6	LLM0_GPLLT_FB_A	T
R2	PL20B	6	LLM0_GPLLC_IN_A**	C*	R2	PL30B	6	LLM0_GPLLC_IN_A**	C*
T4	PL21B	6	LLM0_GPLLC_FB_A	C	T4	PL31B	6	LLM0_GPLLC_FB_A	C
T5	PL23A	6		T	T5	PL33A	6		T
T1	PL22A	6		T*	T1	PL32A	6		T*
T3	PL23B	6		C	T3	PL33B	6		C
GND	GNDIO	6			GND	GNDIO	6		
T2	PL22B	6		C*	T2	PL32B	6		C*
V1	PL25A	6		T	V1	PL39A	6		T
-	-	-			GND	GNDIO	6		
V2	PL25B	6		C	V2	PL39B	6		C
U1	PL24A	6		T*	U1	PL38A	6		T*
U3	PL27A	6		T	U3	PL41A	6		T
U2	PL24B	6		C*	U2	PL38B	6		C*
U4	PL27B	6		C	U4	PL41B	6		C
GND	GNDIO	6			GND	GNDIO	6		
R6	PL26A	6		T*	R6	PL40A	6		T*
R7	PL29A	6		T	R7	PL43A	6		T
T7	PL29B	6		C	T7	PL43B	6		C
T6	PL26B	6		C*	T6	PL40B	6		C*
AA2	PL31A	6		T	AA2	PL45A	6		T
Y1	PL28A	6	LDQS28	T*	Y1	PL42A	6	LDQS42	T*
AA1	PL31B	6		C	AA1	PL45B	6		C
GND	GNDIO	6			GND	GNDIO	6		
W1	PL28B	6		C*	W1	PL42B	6		C*
V3	PL30B	6		C*	V3	PL44B	6		C*
V4	PL30A	6		T*	V4	PL44A	6		T*
U5	TDI	-			U5	TDI	-		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
U7	TCK	-			U7	TCK	-		
V6	TDO	-			V6	TDO	-		
V5	TMS	-			V5	TMS	-		
T8	VCCJ	-			T8	VCCJ	-		
W4	PB3A	5		T	W4	PB3A	5		T
Y3	PB2A	5	VREF2_5	T	Y3	PB2A	5	VREF2_5	T
W3	PB3B	5		C	W3	PB3B	5		C
Y2	PB2B	5	VREF1_5	C	Y2	PB2B	5	VREF1_5	C
AB3	PB5A	5		T	AB3	PB5A	5		T
W5	PB4A	5		T	W5	PB4A	5		T
AB2	PB5B	5		C	AB2	PB5B	5		C
GND	GNDIO	5			GND	GNDIO	5		
W6	PB4B	5		C	W6	PB4B	5		C
AB5	PB7A	5		T	AB5	PB7A	5		T
Y4	PB6A	5	BDQS6	T	Y4	PB6A	5	BDQS6	T
AB4	PB7B	5		C	AB4	PB7B	5		C
AA3	PB6B	5		C	AA3	PB6B	5		C
AB6	PB9A	5		T	AB6	PB9A	5		T
AA5	PB8A	5		T	AA5	PB8A	5		T
AA6	PB9B	5		C	AA6	PB9B	5		C
GND	GNDIO	5			GND	GNDIO	5		
Y5	PB8B	5		C	Y5	PB8B	5		C
Y6	PB12A	5		T	Y6	PB21A	5		T
W7	PB11A	5		T	W7	PB20A	5		T
Y7	PB12B	5		C	Y7	PB21B	5		C
W8	PB11B	5		C	W8	PB20B	5		C
U8	PB14A	5		T	U8	PB23A	5		T
AA7	PB13A	5		T	AA7	PB22A	5		T
U9	PB14B	5		C	U9	PB23B	5		C
AB7	PB13B	5		C	AB7	PB22B	5		C
Y8	PB16A	5		T	Y8	PB25A	5		T
W9	PB15A	5	BDQS15	T	W9	PB24A	5	BDQS24	T
GND	GNDIO	5			GND	GNDIO	5		
AA8	PB16B	5		C	AA8	PB25B	5		C
V9	PB15B	5		C	V9	PB24B	5		C
AB8	PB18A	5		T	AB8	PB27A	5		T
W10	PB17A	5		T	W10	PB26A	5		T
AA9	PB18B	5		C	AA9	PB27B	5		C
GND	GNDIO	5			GND	GNDIO	5		
V10	PB17B	5		C	V10	PB26B	5		C
Y10	PB21A	5		T	Y10	PB30A	5		T
AB9	PB20A	5		T	AB9	PB29A	5		T
AA10	PB21B	5		C	AA10	PB30B	5		C
AB10	PB20B	5		C	AB10	PB29B	5		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AB11	PB23A	5		T	AB11	PB32A	5		T
U10	PB22A	5		T	U10	PB31A	5		T
AA11	PB23B	5		C	AA11	PB32B	5		C
GND	GNDIO	5			GND	GNDIO	5		
U11	PB22B	5		C	U11	PB31B	5		C
AB12	PB25A	5		T	AB12	PB34A	5		T
Y11	PB24A	5	BDQS24	T	Y11	PB33A	5	BDQS33	T
AA12	PB25B	5		C	AA12	PB34B	5		C
W11	PB24B	5		C	W11	PB33B	5		C
AB13	PB26A	5	PCLKT5_0	T	AB13	PB35A	5	PCLKT5_0	T
AB14	PB26B	5	PCLKC5_0	C	AB14	PB35B	5	PCLKC5_0	C
GND	GNDIO	5			GND	GNDIO	5		
Y12	PB32A	4		T	Y12	PB41A	4		T
W12	PB32B	4		C	W12	PB41B	4		C
U12	PB31A	4	PCLKT4_0	T	U12	PB40A	4	PCLKT4_0	T
V12	PB31B	4	PCLKC4_0	C	V12	PB40B	4	PCLKC4_0	C
U13	PB34A	4		T	U13	PB43A	4		T
AA13	PB33A	4	BDQS33	T	AA13	PB42A	4	BDQS42	T
GND	GNDIO	4			GND	GNDIO	4		
U14	PB34B	4		C	U14	PB43B	4		C
Y13	PB33B	4		C	Y13	PB42B	4		C
AB16	PB36A	4		T	AB16	PB45A	4		T
AB15	PB35A	4		T	AB15	PB44A	4		T
AB17	PB36B	4		C	AB17	PB45B	4		C
AA14	PB35B	4		C	AA14	PB44B	4		C
W13	PB37A	4		T	W13	PB46A	4		T
GND	GNDIO	4			GND	GNDIO	4		
W14	PB37B	4		C	W14	PB46B	4		C
AB18	PB39A	4		T	AB18	PB48A	4		T
AB19	PB39B	4		C	AB19	PB48B	4		C
Y15	PB41A	4		T	Y15	PB50A	4		T
V14	PB40A	4		T	V14	PB49A	4		T
AA15	PB41B	4		C	AA15	PB50B	4		C
GND	GNDIO	4			GND	GNDIO	4		
W15	PB40B	4		C	W15	PB49B	4		C
AB20	PB43A	4		T	AB20	PB52A	4		T
AA16	PB42A	4	BDQS42	T	AA16	PB51A	4	BDQS51	T
AB21	PB43B	4		C	AB21	PB52B	4		C
AA17	PB42B	4		C	AA17	PB51B	4		C
Y16	PB45A	4		T	Y16	PB54A	4		T
U15	PB44A	4		T	U15	PB53A	4		T
W16	PB45B	4		C	W16	PB54B	4		C
U16	PB44B	4		C	U16	PB53B	4		C
AA18	PB46A	4		T	AA18	PB55A	4		T

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AA20	PB46B	4		C	AA20	PB55B	4		C
GND	GNDIO	4			GND	GNDIO	4		
V16	PB49A	4		T	V16	PB58A	4		T
V17	PB49B	4		C	V17	PB58B	4		C
AA21	PB48A	4		T	AA21	PB57A	4		T
Y19	PB51A	4	BDQS51	T	Y19	PB60A	4	BDQS60	T
GND	GNDIO	4			GND	GNDIO	4		
AA22	PB48B	4		C	AA22	PB57B	4		C
Y20	PB51B	4		C	Y20	PB60B	4		C
Y18	PB50A	4		T	Y18	PB59A	4		T
Y21	PB53A	4		T	Y21	PB62A	4		T
Y17	PB50B	4		C	Y17	PB59B	4		C
Y22	PB53B	4		C	Y22	PB62B	4		C
W17	PB52A	4		T	W17	PB61A	4		T
U18	PB54A	4		T	U18	PB63A	4		T
W18	PB52B	4		C	W18	PB61B	4		C
V18	PB54B	4		C	V18	PB63B	4		C
GND	GNDIO	4			GND	GNDIO	4		
T15	PB55A	4	VREF2_4	T	T15	PB64A	4	VREF2_4	T
T16	PB55B	4	VREF1_4	C	T16	PB64B	4	VREF1_4	C
W19	CFG2	8			W19	CFG2	8		
V19	CFG1	8			V19	CFG1	8		
V20	PROGRAMN	8			V20	PROGRAMN	8		
W20	CFG0	8			W20	CFG0	8		
U22	PR28B	8	D1	C	U22	PR42B	8	D1	C
V22	INITN	8			V22	INITN	8		
R16	PR30B	8	WRITEN	C	R16	PR44B	8	WRITEN	C
GND	GNDIO	8			GND	GNDIO	8		
W22	CCLK	8			W22	CCLK	8		
R17	PR30A	8	CS1N	T	R17	PR44A	8	CS1N	T
V21	DONE	8			V21	DONE	8		
U19	PR29B	8	CSN	C	U19	PR43B	8	CSN	C
T17	PR26B	8	D5	C	T17	PR40B	8	D5	C
U20	PR29A	8	D0	T	U20	PR43A	8	D0	T
U21	PR28A	8	D2	T	U21	PR42A	8	D2	T
T18	PR26A	8	D6	T	T18	PR40A	8	D6	T
T20	PR27B	8	D3	C	T20	PR41B	8	D3	C
GND	GNDIO	8			GND	GNDIO	8		
T21	PR25B	8	D7	C	T21	PR39B	8	D7	C
T19	PR27A	8	D4	T	T19	PR41A	8	D4	T
T22	PR25A	8	DI	T	T22	PR39A	8	DI	T
R18	PR24B	8	DOUT,CSON	C	R18	PR38B	8	DOUT,CSON	C
R19	PR24A	8	BUSY	T	R19	PR38A	8	BUSY	T
GND	GNDIO	8			GND	GNDIO	8		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P18	PR22B	3		C*	P18	PR32B	3		C*
GND	GNDIO	3			GND	GNDIO	3		
R22	PR23B	3		C	R22	PR33B	3		C
P19	PR22A	3		T*	P19	PR32A	3		T*
R21	PR23A	3		T	R21	PR33A	3		T
R20	PR21B	3	RLM0_GPLLC_FB_A	C	R20	PR31B	3	RLM0_GPLLC_FB_A	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	P22	PR31A	3	RLM0_GPLLT_FB_A	T
P21	PR20B	3	RLM0_GPLLC_IN_A**	C*	P21	PR30B	3	RLM0_GPLLC_IN_A**	C*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T*	N21	PR30A	3	RLM0_GPLLT_IN_A**	T*
N17	RLM0_PLLCAP	3			N17	RLM0_PLLCAP	3		
N18	VCC	-			N18	VCC	-		
N22	PR18B	3	RLM0_GDLLC_FB_A	C	N22	PR28B	3	RLM0_GDLLC_FB_A	C
M22	PR17B	3	RLM0_GDLLC_IN_A**	C*	M22	PR27B	3	RLM0_GDLLC_IN_A**	C*
GND	GNDIO	3			GND	GNDIO	3		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	N20	PR28A	3	RLM0_GDLLT_FB_A	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T*	M21	PR27A	3	RLM0_GDLLT_IN_A**	T*
N19	NC	-			N19	PR26B	3		C
M19	NC	-			M19	PR26A	3		T
J22	NC	-			J22	PR23B	3		C*
-	-	-			GND	GNDIO	3		
L22	NC	-			L22	PR24B	3		C
H22	NC	-			H22	PR23A	3		T*
K22	NC	-			K22	PR24A	3		T
M20	PR16B	3	VREF2_3	C	M20	PR22B	3	VREF2_3	C
L21	PR16A	3	VREF1_3	T	L21	PR22A	3	VREF1_3	T
K21	PR15B	3	PCLKC3_0	C*	K21	PR21B	3	PCLKC3_0	C*
J21	PR15A	3	PCLKT3_0	T*	J21	PR21A	3	PCLKT3_0	T*
M18	PR13B	2	PCLKC2_0	C	M18	PR19B	2	PCLKC2_0	C
GND	GNDIO	2			GND	GNDIO	2		
L17	PR13A	2	PCLKT2_0	T	L17	PR19A	2	PCLKT2_0	T
L19	PR12B	2		C*	L19	PR18B	2		C*
K18	PR10B	2		C*	K18	PR16B	2		C*
L20	PR12A	2		T*	L20	PR18A	2		T*
K19	PR10A	2	RDQS10	T*	K19	PR16A	2	RDQS16	T*
GND	GNDIO	2			GND	GNDIO	2		
L18	PR11B	2		C	L18	PR17B	2		C
K17	PR11A	2		T	K17	PR17A	2		T
J16	NC	-			J16	NC	-		
J17	PR8B	2		C*	J17	PR14B	2		C*
G22	PR9B	2		C	G22	PR15B	2		C
J18	PR8A	2		T*	J18	PR14A	2		T*
F22	PR9A	2		T	F22	PR15A	2		T
H21	PR6B	2		C*	H21	PR12B	2		C*
K20	PR7B	2		C	K20	PR13B	2		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
G21	PR6A	2		T*	G21	PR12A	2		T*
J19	PR7A	2		T	J19	PR13A	2		T
D22	NC	-			D22	PR10B	2		C*
F21	NC	-			F21	PR11B	2		C
-	-	-			GND	GNDIO	2		
E21	NC	-			E21	PR10A	2		T*
E22	NC	-			E22	PR11A	2		T
H19	NC	-			H19	PR8B	2		C*
G20	NC	-			G20	PR9B	2		C
G19	NC	-			G19	PR8A	2	RDQS8	T*
F20	NC	-			F20	PR9A	2		T
G17	PR5B	2		C	G17	PR7B	2		C
GND	GNDIO	2			GND	GNDIO	2		
E20	PR4B	2		C*	E20	PR6B	2		C*
F19	PR5A	2		T	F19	PR7A	2		T
D20	PR4A	2		T*	D20	PR6A	2		T*
F18	PR3B	2		C	F18	PR5B	2		C
C21	NC	-			C21	PR4B	2		C*
F16	PR3A	2		T	F16	PR5A	2		T
C22	NC	-			C22	PR4A	2		T*
-	-	-			GND	GNDIO	2		
D19	PR2B	2	VREF2_2	C*	D19	PR2B	2	VREF2_2	C*
E19	PR2A	2	VREF1_2	T*	E19	PR2A	2	VREF1_2	T*
B21	PT55B	1	VREF2_1	C	B21	PT64B	1	VREF2_1	C
B22	PT55A	1	VREF1_1	T	B22	PT64A	1	VREF1_1	T
GND	GNDIO	1			GND	GNDIO	1		
D18	PT53B	1		C	D18	PT62B	1		C
C20	PT54B	1		C	C20	PT63B	1		C
E18	PT53A	1		T	E18	PT62A	1		T
C19	PT54A	1		T	C19	PT63A	1		T
B20	PT52B	1		C	B20	PT61B	1		C
D17	PT51B	1		C	D17	PT60B	1		C
C18	PT51A	1		T	C18	PT60A	1		T
GND	GNDIO	1			GND	GNDIO	1		
A19	PT52A	1		T	A19	PT61A	1		T
A18	PT49B	1		C	A18	PT58B	1		C
A21	PT50B	1		C	A21	PT59B	1		C
B18	PT49A	1		T	B18	PT58A	1		T
A20	PT50A	1		T	A20	PT59A	1		T
D16	PT47B	1		C	D16	PT56B	1		C
G16	PT48B	1		C	G16	PT57B	1		C
E16	PT47A	1		T	E16	PT56A	1		T
G15	PT48A	1		T	G15	PT57A	1		T
C17	PT46B	1		C	C17	PT55B	1		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	1			GND	GNDIO	1		
C16	PT46A	1		T	C16	PT55A	1		T
A17	PT44B	1		C	A17	PT53B	1		C
B17	PT45B	1		C	B17	PT54B	1		C
A16	PT44A	1		T	A16	PT53A	1		T
B16	PT45A	1		T	B16	PT54A	1		T
E15	PT42B	1		C	E15	PT51B	1		C
C15	PT43B	1		C	C15	PT52B	1		C
F15	PT42A	1		T	F15	PT51A	1		T
GND	GNDIO	1			GND	GNDIO	1		
D15	PT43A	1		T	D15	PT52A	1		T
B15	PT40B	1		C	B15	PT49B	1		C
A15	PT40A	1		T	A15	PT49A	1		T
A14	PT39A	1		T	A14	PT48A	1		T
B14	PT39B	1		C	B14	PT48B	1		C
D14	PT37B	1		C	D14	PT46B	1		C
E14	PT36B	1		C	E14	PT45B	1		C
C13	PT37A	1		T	C13	PT46A	1		T
GND	GNDIO	1			GND	GNDIO	1		
F14	PT36A	1		T	F14	PT45A	1		T
A13	PT35B	1		C	A13	PT44B	1		C
E13	PT34B	1		C	E13	PT43B	1		C
B13	PT35A	1		T	B13	PT44A	1		T
D13	PT34A	1		T	D13	PT43A	1		T
E12	PT33B	1		C	E12	PT42B	1		C
D12	PT33A	1		T	D12	PT42A	1		T
GND	GNDIO	1			GND	GNDIO	1		
A12	PT31B	1		C	A12	PT40B	1		C
B12	PT30B	1	PCLKC1_0	C	B12	PT39B	1	PCLKC1_0	C
A11	PT31A	1		T	A11	PT40A	1		T
C12	PT30A	1	PCLKT1_0	T	C12	PT39A	1	PCLKT1_0	T
F12	XRES	1			F12	XRES	1		
GND	GNDIO	0			GND	GNDIO	0		
B10	PT28B	0	PCLKC0_0	C	B10	PT37B	0	PCLKC0_0	C
B11	PT28A	0	PCLKT0_0	T	B11	PT37A	0	PCLKT0_0	T
C11	PT26B	0		C	C11	PT35B	0		C
A10	PT27B	0		C	A10	PT36B	0		C
C10	PT26A	0		T	C10	PT35A	0		T
A9	PT27A	0		T	A9	PT36A	0		T
A8	PT24B	0		C	A8	PT33B	0		C
E11	PT25B	0		C	E11	PT34B	0		C
A7	PT24A	0		T	A7	PT33A	0		T
F11	PT25A	0		T	F11	PT34A	0		T
B8	PT23B	0		C	B8	PT32B	0		C

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	0			GND	GNDIO	0		
B9	PT23A	0		T	B9	PT32A	0		T
C8	PT20B	0		C	C8	PT29B	0		C
B7	PT21B	0		C	B7	PT30B	0		C
D8	PT20A	0		T	D8	PT29A	0		T
GND	GNDIO	0			GND	GNDIO	0		
A6	PT21A	0		T	A6	PT30A	0		T
C7	PT17B	0		C	C7	PT26B	0		C
D10	PT18B	0		C	D10	PT27B	0		C
C6	PT17A	0		T	C6	PT26A	0		T
E10	PT18A	0		T	E10	PT27A	0		T
F10	PT15B	0		C	F10	PT24B	0		C
B6	PT16B	0		C	B6	PT25B	0		C
D9	PT15A	0		T	D9	PT24A	0		T
B5	PT16A	0		T	B5	PT25A	0		T
GND	GNDIO	0			GND	GNDIO	0		
A5	PT13B	0		C	A5	PT22B	0		C
F9	PT14B	0		C	F9	PT23B	0		C
A4	PT13A	0		T	A4	PT22A	0		T
E9	PT14A	0		T	E9	PT23A	0		T
G8	PT11B	0		C	G8	PT20B	0		C
A3	PT12B	0		C	A3	PT21B	0		C
E8	PT11A	0		T	E8	PT20A	0		T
A2	PT12A	0		T	A2	PT21A	0		T
C3	PT10B	0		C	C3	PT10B	0		C
GND	GNDIO	0			GND	GNDIO	0		
B3	PT10A	0		T	B3	PT10A	0		T
E7	PT8B	0		C	E7	PT8B	0		C
F8	PT9B	0		C	F8	PT9B	0		C
F7	PT8A	0		T	F7	PT8A	0		T
D7	PT9A	0		T	D7	PT9A	0		T
D4	PT6B	0		C	D4	PT6B	0		C
D5	PT7B	0		C	D5	PT7B	0		C
C4	PT6A	0		T	C4	PT6A	0		T
D6	PT7A	0		T	D6	PT7A	0		T
J7	PT4B	0		C	J7	PT4B	0		C
B2	PT5B	0		C	B2	PT5B	0		C
GND	GNDIO	0			GND	GNDIO	0		
H7	PT4A	0		T	H7	PT4A	0		T
B1	PT5A	0		T	B1	PT5A	0		T
D1	PT2B	0	VREF2_0	C	D1	PT2B	0	VREF2_0	C
D3	PT3B	0		C	D3	PT3B	0		C
C1	PT2A	0	VREF1_0	T	C1	PT2A	0	VREF1_0	T
C2	PT3A	0		T	C2	PT3A	0		T

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J10	VCC	-			J10	VCC	-		
J11	VCC	-			J11	VCC	-		
J12	VCC	-			J12	VCC	-		
J13	VCC	-			J13	VCC	-		
K14	VCC	-			K14	VCC	-		
K9	VCC	-			K9	VCC	-		
L14	VCC	-			L14	VCC	-		
L9	VCC	-			L9	VCC	-		
M14	VCC	-			M14	VCC	-		
M9	VCC	-			M9	VCC	-		
N14	VCC	-			N14	VCC	-		
N9	VCC	-			N9	VCC	-		
P10	VCC	-			P10	VCC	-		
P11	VCC	-			P11	VCC	-		
P12	VCC	-			P12	VCC	-		
P13	VCC	-			P13	VCC	-		
G10	VCCIO0	0			G10	VCCIO0	0		
G9	VCCIO0	0			G9	VCCIO0	0		
H8	VCCIO0	0			H8	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0		
G11	VCCIO1	1			G11	VCCIO1	1		
G12	VCCIO1	1			G12	VCCIO1	1		
G13	VCCIO1	1			G13	VCCIO1	1		
G14	VCCIO1	1			G14	VCCIO1	1		
H14	VCCIO2	2			H14	VCCIO2	2		
H15	VCCIO2	2			H15	VCCIO2	2		
J15	VCCIO2	2			J15	VCCIO2	2		
K16	VCCIO2	2			K16	VCCIO2	2		
L16	VCCIO3	3			L16	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3		
N16	VCCIO3	3			N16	VCCIO3	3		
P16	VCCIO3	3			P16	VCCIO3	3		
R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4		
T13	VCCIO4	4			T13	VCCIO4	4		
T14	VCCIO4	4			T14	VCCIO4	4		
R9	VCCIO5	5			R9	VCCIO5	5		
T10	VCCIO5	5			T10	VCCIO5	5		
T11	VCCIO5	5			T11	VCCIO5	5		
T9	VCCIO5	5			T9	VCCIO5	5		
N7	VCCIO6	6			N7	VCCIO6	6		
P7	VCCIO6	6			P7	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J8	VCCIO7	7			J8	VCCIO7	7		
K7	VCCIO7	7			K7	VCCIO7	7		
L7	VCCIO7	7			L7	VCCIO7	7		
M7	VCCIO7	7			M7	VCCIO7	7		
P15	VCCIO8	8			P15	VCCIO8	8		
R15	VCCIO8	8			R15	VCCIO8	8		
C5	VCCAUX	-			C5	VCCAUX	-		
D11	VCCAUX	-			D11	VCCAUX	-		
E17	VCCAUX	-			E17	VCCAUX	-		
E6	VCCAUX	-			E6	VCCAUX	-		
F13	VCCAUX	-			F13	VCCAUX	-		
G18	VCCAUX	-			G18	VCCAUX	-		
G5	VCCAUX	-			G5	VCCAUX	-		
K5	VCCAUX	-			K5	VCCAUX	-		
M17	VCCAUX	-			M17	VCCAUX	-		
P17	VCCAUX	-			P17	VCCAUX	-		
R5	VCCAUX	-			R5	VCCAUX	-		
V11	VCCAUX	-			V11	VCCAUX	-		
V13	VCCAUX	-			V13	VCCAUX	-		
V15	VCCAUX	-			V15	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
V8	VCCAUX	-			V8	VCCAUX	-		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		
AA19	GND	-			AA19	GND	-		
AA4	GND	-			AA4	GND	-		
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
B19	GND	-			B19	GND	-		
B4	GND	-			B4	GND	-		
C14	GND	-			C14	GND	-		
C9	GND	-			C9	GND	-		
D2	GND	-			D2	GND	-		
D21	GND	-			D21	GND	-		
F17	GND	-			F17	GND	-		
F6	GND	-			F6	GND	-		
H10	GND	-			H10	GND	-		
H11	GND	-			H11	GND	-		
H12	GND	-			H12	GND	-		
H13	GND	-			H13	GND	-		
J14	GND	-			J14	GND	-		
J20	GND	-			J20	GND	-		
J3	GND	-			J3	GND	-		
J9	GND	-			J9	GND	-		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K15	GND	-			K15	GND	-		
K8	GND	-			K8	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L15	GND	-			L15	GND	-		
L8	GND	-			L8	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M15	GND	-			M15	GND	-		
M8	GND	-			M8	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N15	GND	-			N15	GND	-		
N8	GND	-			N8	GND	-		
P14	GND	-			P14	GND	-		
P20	GND	-			P20	GND	-		
P3	GND	-			P3	GND	-		
P9	GND	-			P9	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
U17	GND	-			U17	GND	-		
U6	GND	-			U6	GND	-		
W2	GND	-			W2	GND	-		
W21	GND	-			W21	GND	-		
Y14	GND	-			Y14	GND	-		
Y9	GND	-			Y9	GND	-		
H6	NC	-			H6	NC	-		
J6	NC	-			J6	NC	-		
H3	NC	-			H3	NC	-		
H2	NC	-			H2	NC	-		
H17	NC	-			H17	NC	-		
H16	NC	-			H16	NC	-		

LFE2-12E/12SE and LFE2-20E/20SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
H20	NC	-			H20	NC	-		
H18	NC	-			H18	NC	-		

* Supports true LVDS outputs.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E4	PL2A	7	VREF2_7	T*	E4	PL2A	7	VREF2_7	T*
E5	PL2B	7	VREF1_7	C*	E5	PL2B	7	VREF1_7	C*
GND	GNDIO	7			GND	GNDIO	7		
E3	PL10A	7		T*	E3	PL12A	7		T*
F4	PL11A	7		T	F4	PL13A	7		T
F3	PL10B	7		C*	F3	PL12B	7		C*
F5	PL11B	7		C	F5	PL13B	7		C
E2	PL12A	7		T*	E2	PL14A	7		T*
G6	PL13A	7		T	G6	PL15A	7		T
E1	PL12B	7		C*	E1	PL14B	7		C*
G7	PL13B	7		C	G7	PL15B	7		C
GND	GNDIO	7			GND	GNDIO	7		
F1	PL15A	7		T	F1	PL17A	7		T
H4	PL14A	7	LDQS14	T*	H4	PL16A	7	LDQS16	T*
F2	PL15B	7		C	F2	PL17B	7		C
H5	PL14B	7		C*	H5	PL16B	7		C*
G1	PL17A	7		T	G1	PL19A	7		T
G3	PL16A	7		T*	G3	PL18A	7		T*
G2	PL17B	7		C	G2	PL19B	7		C
GND	GNDIO	7			GND	GNDIO	7		
G4	PL16B	7		C*	G4	PL18B	7		C*
J4	PL19A	7		T	J4	PL38A	7		T
H1	PL18A	7			H1	PL37A	7		
J5	PL19B	7		C	J5	PL38B	7		C
L6	PL21A	7		T	L6	PL40A	7		T
J2	PL20A	7		T*	J2	PL39A	7		T*
L5	PL21B	7		C	L5	PL40B	7		C
J1	PL20B	7		C*	J1	PL39B	7		C*
K3	PL22A	7	LDQS22	T*	K3	PL41A	7	LDQS41	T*
GND	GNDIO	7			GND	GNDIO	7		
K6	NC	-			K6	VCCPLL	-		
K4	PL22B	7		C*	K4	PL41B	7		C*
K2	PL23A	7		T	K2	PL42A	7		T
K1	PL23B	7		C	K1	PL42B	7		C
L4	PL24A	7		T*	L4	PL43A	7		T*
L3	PL24B	7		C*	L3	PL43B	7		C*
GND	GNDIO	7			GND	GNDIO	7		
L2	PL25A	7	PCLKT7_0	T	L2	PL44A	7	PCLKT7_0	T
L1	PL25B	7	PCLKC7_0	C	L1	PL44B	7	PCLKC7_0	C
M5	PL27A	6	PCLKT6_0	T*	M5	PL46A	6	PCLKT6_0	T*
M6	PL27B	6	PCLKC6_0	C*	M6	PL46B	6	PCLKC6_0	C*
M3	PL28A	6	VREF2_6	T	M3	PL47A	6	VREF2_6	T
M4	PL28B	6	VREF1_6	C	M4	PL47B	6	VREF1_6	C
N1	PL30A	6		T	N1	PL49A	6		T

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
M2	PL29A	6		T*	M2	PL48A	6		T*
N2	PL30B	6		C	N2	PL49B	6		C
M1	PL29B	6		C*	M1	PL48B	6		C*
GND	GNDIO	6			GND	GNDIO	6		
N3	PL39A	6	LDQS39	T*	N3	PL58A	6	LDQS58	T*
N5	PL40A	6		T	N5	PL59A	6		T
N4	PL39B	6		C*	N4	PL58B	6		C*
P5	PL40B	6		C	P5	PL59B	6		C
P1	PL41A	6	LLM0_GDLLT_IN_A**	T*	P1	PL60A	6	LLM0_GDLLT_IN_A**	T*
P2	PL41B	6	LLM0_GDLLC_IN_A**	C*	P2	PL60B	6	LLM0_GDLLC_IN_A**	C*
P4	PL42A	6	LLM0_GDLLT_FB_A	T	P4	PL61A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO	6			GND	GNDIO	6		
R4	PL42B	6	LLM0_GDLLC_FB_A	C	R4	PL61B	6	LLM0_GDLLC_FB_D	C
N6	VCCPLL	-			N6	VCCPLL	-		
P6	LLM0_PLLCAP	6			P6	LLM0_PLLCAP	6		
R1	PL44A	6	LLM0_GPLLT_IN_A**	T*	R1	PL63A	6	LLM0_GPLLT_IN_A**	T*
R3	PL45A	6	LLM0_GPLLT_FB_A	T	R3	PL64A	6	LLM0_GPLLT_FB_A	T
R2	PL44B	6	LLM0_GPLLC_IN_A**	C*	R2	PL63B	6	LLM0_GPLLC_IN_A**	C*
T4	PL45B	6	LLM0_GPLLC_FB_A	C	T4	PL64B	6	LLM0_GPLLC_FB_A	C
T5	PL47A	6		T	T5	PL66A	6		T
T1	PL46A	6		T*	T1	PL65A	6		T*
T3	PL47B	6		C	T3	PL66B	6		C
GND	GNDIO	6			GND	GNDIO	6		
T2	PL46B	6		C*	T2	PL65B	6		C*
V1	PL53A	6		T	V1	PL72A	6		T
GND	GNDIO	6			GND	GNDIO	6		
V2	PL53B	6		C	V2	PL72B	6		C
U1	PL52A	6		T*	U1	PL71A	6		T*
U3	PL55A	6		T	U3	PL74A	6		T
U2	PL52B	6		C*	U2	PL71B	6		C*
U4	PL55B	6		C	U4	PL74B	6		C
GND	GNDIO	6			GND	GNDIO	6		
R6	PL54A	6		T*	R6	PL73A	6		T*
R7	PL57A	6		T	R7	PL76A	6		T
T7	PL57B	6		C	T7	PL76B	6		C
T6	PL54B	6		C*	T6	PL73B	6		C*
AA2	PL59A	6		T	AA2	PL78A	6		T
Y1	PL56A	6	LDQS56	T*	Y1	PL75A	6	LDQS75	T*
AA1	PL59B	6		C	AA1	PL78B	6		C
GND	GNDIO	6			GND	GNDIO	6		
W1	PL56B	6		C*	W1	PL75B	6		C*
V3	PL58B	6		C*	V3	PL77B	6		C*
V4	PL58A	6		T*	V4	PL77A	6		T*
U5	TDI	-			U5	TDI	-		

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
U7	TCK	-			U7	TCK	-		
V6	TDO	-			V6	TDO	-		
V5	TMS	-			V5	TMS	-		
T8	VCCJ	-			T8	VCCJ	-		
W4	PB3A	5		T	W4	PB3A	5		T
Y3	PB2A	5	VREF2_5	T	Y3	PB2A	5	VREF2_5	T
W3	PB3B	5		C	W3	PB3B	5		C
Y2	PB2B	5	VREF1_5	C	Y2	PB2B	5	VREF1_5	C
AB3	PB5A	5		T	AB3	PB5A	5		T
W5	PB4A	5		T	W5	PB4A	5		T
AB2	PB5B	5		C	AB2	PB5B	5		C
GND	GNDIO	5			GND	GNDIO	5		
W6	PB4B	5		C	W6	PB4B	5		C
AB5	PB7A	5		T	AB5	PB7A	5		T
Y4	PB6A	5	BDQS6	T	Y4	PB6A	5	BDQS6	T
AB4	PB7B	5		C	AB4	PB7B	5		C
AA3	PB6B	5		C	AA3	PB6B	5		C
AB6	PB9A	5		T	AB6	PB9A	5		T
AA5	PB8A	5		T	AA5	PB8A	5		T
AA6	PB9B	5		C	AA6	PB9B	5		C
GND	GNDIO	5			GND	GNDIO	5		
Y5	PB8B	5		C	Y5	PB8B	5		C
Y6	PB21A	5		T	Y6	PB30A	5		T
W7	PB20A	5		T	W7	PB29A	5		T
Y7	PB21B	5		C	Y7	PB30B	5		C
W8	PB20B	5		C	W8	PB29B	5		C
U8	PB23A	5		T	U8	PB32A	5		T
AA7	PB22A	5		T	AA7	PB31A	5		T
U9	PB23B	5		C	U9	PB32B	5		C
AB7	PB22B	5		C	AB7	PB31B	5		C
Y8	PB25A	5		T	Y8	PB34A	5		T
W9	PB24A	5	BDQS24	T	W9	PB33A	5	BDQS33	T
GND	GNDIO	5			GND	GNDIO	5		
AA8	PB25B	5		C	AA8	PB34B	5		C
V9	PB24B	5		C	V9	PB33B	5		C
AB8	PB27A	5		T	AB8	PB36A	5		T
W10	PB26A	5		T	W10	PB35A	5		T
AA9	PB27B	5		C	AA9	PB36B	5		C
GND	GNDIO	5			GND	GNDIO	5		
V10	PB26B	5		C	V10	PB35B	5		C
Y10	PB30A	5		T	Y10	PB39A	5		T
AB9	PB29A	5		T	AB9	PB38A	5		T
AA10	PB30B	5		C	AB10	PB38B	5		C
AB10	PB29B	5		C	AA10	PB39B	5		C

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AB11	PB32A	5		T	AB11	PB41A	5		T
U10	PB31A	5		T	U10	PB40A	5		T
AA11	PB32B	5		C	AA11	PB41B	5		C
GND	GNDIO	5			GND	GNDIO	5		
U11	PB31B	5		C	U11	PB40B	5		C
AB12	PB34A	5		T	AB12	PB43A	5		T
Y11	PB33A	5	BDQS33	T	Y11	PB42A	5	BDQS42	T
AA12	PB34B	5		C	AA12	PB43B	5		C
W11	PB33B	5		C	W11	PB42B	5		C
AB13	PB35A	5	PCLKT5_0	T	AB13	PB44A	5	PCLKT5_0	T
AB14	PB35B	5	PCLKC5_0	C	AB14	PB44B	5	PCLKC5_0	C
GND	GNDIO	5			GND	GNDIO	5		
Y12	PB41A	4		T	Y12	PB50A	4		T
W12	PB41B	4		C	W12	PB50B	4		C
U12	PB40A	4	PCLKT4_0	T	U12	PB49A	4	PCLKT4_0	T
V12	PB40B	4	PCLKC4_0	C	V12	PB49B	4	PCLKC4_0	C
U13	PB43A	4		T	U13	PB52A	4		T
AA13	PB42A	4	BDQS42	T	AA13	PB51A	4	BDQS51	T
GND	GNDIO	4			GND	GNDIO	4		
U14	PB43B	4		C	U14	PB52B	4		C
Y13	PB42B	4		C	Y13	PB51B	4		C
AB16	PB45A	4		T	AB16	PB54A	4		T
AB15	PB44A	4		T	AB15	PB53A	4		T
AB17	PB45B	4		C	AB17	PB54B	4		C
AA14	PB44B	4		C	AA14	PB53B	4		C
W13	PB46A	4		T	W13	PB55A	4		T
GND	GNDIO	4			GND	GNDIO	4		
W14	PB46B	4		C	W14	PB55B	4		C
AB18	PB48A	4		T	AB18	PB57A	4		T
AB19	PB48B	4		C	AB19	PB57B	4		C
Y15	PB50A	4		T	Y15	PB59A	4		T
V14	PB49A	4		T	V14	PB58A	4		T
AA15	PB50B	4		C	AA15	PB59B	4		C
GND	GNDIO	4			GND	GNDIO	4		
W15	PB49B	4		C	W15	PB58B	4		C
AB20	PB52A	4		T	AB20	PB61A	4		T
AA16	PB51A	4	BDQS51	T	AA16	PB60A	4	BDQS60	T
AB21	PB52B	4		C	AB21	PB61B	4		C
AA17	PB51B	4		C	AA17	PB60B	4		C
Y16	PB54A	4		T	Y16	PB63A	4		T
U15	PB53A	4		T	U15	PB62A	4		T
W16	PB54B	4		C	W16	PB63B	4		C
U16	PB53B	4		C	U16	PB62B	4		C
AA18	PB55A	4		T	AA18	PB64A	4		T

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AA20	PB55B	4		C	AA20	PB64B	4		C
GND	GNDIO	4			GND	GNDIO	4		
V16	PB67A	4		T	V16	PB76A	4		T
V17	PB67B	4		C	V17	PB76B	4		C
AA21	PB66A	4		T	AA21	PB75A	4		T
Y19	PB69A	4	BDQS69	T	Y19	PB78A	4	BDQS78	T
GND	GNDIO	4			GND	GNDIO	4		
AA22	PB66B	4		C	AA22	PB75B	4		C
Y20	PB69B	4		C	Y20	PB78B	4		C
Y18	PB68A	4		T	Y18	PB77A	4		T
Y21	PB71A	4		T	Y21	PB80A	4		T
Y17	PB68B	4		C	Y17	PB77B	4		C
Y22	PB71B	4		C	Y22	PB80B	4		C
W17	PB70A	4		T	W17	PB79A	4		T
U18	PB72A	4		T	U18	PB81A	4		T
W18	PB70B	4		C	W18	PB79B	4		C
V18	PB72B	4		C	V18	PB81B	4		C
GND	GNDIO	4			GND	GNDIO	4		
T15	PB73A	4	VREF2_4	T	T15	PB82A	4	VREF2_4	T
T16	PB73B	4	VREF1_4	C	T16	PB82B	4	VREF1_4	C
W19	CFG2	8			W19	CFG2	8		
V19	CFG1	8			V19	CFG1	8		
V20	PROGRAMN	8			V20	PROGRAMN	8		
W20	CFG0	8			W20	CFG0	8		
U22	PR56B	8	D1	C	U22	PR75B	8	D1	C
V22	INITN	8			V22	INITN	8		
R16	PR58B	8	WRITEN	C	R16	PR77B	8	WRITEN	C
GND	GNDIO	8			GND	GNDIO	8		
W22	CCLK	8			W22	CCLK	8		
R17	PR58A	8	CS1N	T	R17	PR77A	8	CS1N	T
V21	DONE	8			V21	DONE	8		
U19	PR57B	8	CSN	C	U19	PR76B	8	CSN	C
T17	PR54B	8	D5	C	T17	PR73B	8	D5	C
U20	PR57A	8	D0	T	U20	PR76A	8	D0	T
U21	PR56A	8	D2	T	U21	PR75A	8	D2	T
T18	PR54A	8	D6	T	T18	PR73A	8	D6	T
T20	PR55B	8	D3	C	T20	PR74B	8	D3	C
GND	GNDIO	8			GND	GNDIO	8		
T21	PR53B	8	D7	C	T21	PR72B	8	D7	C
T19	PR55A	8	D4	T	T19	PR74A	8	D4	T
T22	PR53A	8	DI	T	T22	PR72A	8	DI	T
R18	PR52B	8	DOUT_CSON	C	R18	PR71B	8	DOUT,CSON	C
R19	PR52A	8	BUSY	T	R19	PR71A	8	BUSY	T
GND	GNDIO	8			GND	GNDIO	8		

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P18	PR46B	3		C*	P18	PR65B	3		C*
GND	GNDIO	3			GND	GNDIO	3		
R22	PR47B	3		C	R22	PR66B	3		C
P19	PR46A	3		T*	P19	PR65A	3		T*
R21	PR47A	3		T	R21	PR66A	3		T
R20	PR45B	3	RLM0_GPLLC_FB_A	C	R20	PR64B	3	RLM0_GPLLC_FB_A	C
P22	PR45A	3	RLM0_GPLLT_FB_A	T	P22	PR64A	3	RLM0_GPLLT_FB_A	T
P21	PR44B	3	RLM0_GPLLC_IN_A**	C*	P21	PR63B	3	RLM0_GPLLC_IN_A**	C*
N21	PR44A	3	RLM0_GPLLT_IN_A**	T*	N21	PR63A	3	RLM0_GPLLT_IN_A**	T*
N17	RLM0_PLLCAP	3			N17	RLM0_PLLCAP	3		
N18	VCCPLL	-			N18	VCCPLL	-		
N22	PR42B	3	RLM0_GDLLC_FB_A	C	N22	PR61B	3	RLM0_GDLLC_FB_A	C
M22	PR41B	3	RLM0_GDLLC_IN_A**	C*	M22	PR60B	3	RLM0_GDLLC_IN_A**	C*
GND	GNDIO	3			GND	GNDIO	3		
N20	PR42A	3	RLM0_GDLLT_FB_A	T	N20	PR61A	3	RLM0_GDLLT_FB_A	T
M21	PR41A	3	RLM0_GDLLT_IN_A**	T*	M21	PR60A	3	RLM0_GDLLT_IN_A**	T*
N19	PR40B	3		C	N19	PR59B	3		C
M19	PR40A	3		T	M19	PR59A	3		T
J22	PR29B	3		C*	J22	PR48B	3		C*
GND	GNDIO	3			GND	GNDIO	3		
L22	PR30B	3		C	L22	PR49B	3		C
H22	PR29A	3		T*	H22	PR48A	3		T*
K22	PR30A	3		T	K22	PR49A	3		T
M20	PR28B	3	VREF2_3	C	M20	PR47B	3	VREF2_3	C
L21	PR28A	3	VREF1_3	T	L21	PR47A	3	VREF1_3	T
K21	PR27B	3	PCLKC3_0	C*	K21	PR46B	3	PCLKC3_0	C*
J21	PR27A	3	PCLKT3_0	T*	J21	PR46A	3	PCLKT3_0	T*
M18	PR25B	2	PCLKC2_0	C	M18	PR44B	2	PCLKC2_0	C
GND	GNDIO	2			GND	GNDIO	2		
L17	PR25A	2	PCLKT2_0	T	L17	PR44A	2	PCLKT2_0	T
L19	PR24B	2		C*	L19	PR43B	2		C*
K18	PR22B	2		C*	K18	PR41B	2		C*
L20	PR24A	2		T*	L20	PR43A	2		T*
K19	PR22A	2	RDQS22	T*	K19	PR41A	2	RDQS41	T*
GND	GNDIO	2			GND	GNDIO	2		
L18	PR23B	2		C	L18	PR42B	2		C
K17	PR23A	2		T	K17	PR42A	2		T
J16	NC	-			J16	VCCPLL	-		
J17	PR20B	2		C*	J17	PR39B	2		C*
G22	PR21B	2		C	G22	PR40B	2		C
J18	PR20A	2		T*	J18	PR39A	2		T*
F22	PR21A	2		T	F22	PR40A	2		T
H21	PR18B	2		C*	H21	PR37B	2		C*
K20	PR19B	2		C	K20	PR38B	2		C

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
G21	PR18A	2		T*	G21	PR37A	2		T*
J19	PR19A	2		T	J19	PR38A	2		T
D22	PR16B	2		C*	D22	PR18B	2		C*
F21	PR17B	2		C	F21	PR19B	2		C
GND	GNDIO	2			GND	GNDIO	2		
E21	PR16A	2		T*	E21	PR18A	2		T*
E22	PR17A	2		T	E22	PR19A	2		T
H19	PR14B	2		C*	H19	PR16B	2		C*
G20	PR15B	2		C	G20	PR17B	2		C
G19	PR14A	2	RDQS14	T*	G19	PR16A	2	RDQS16	T*
F20	PR15A	2		T	F20	PR17A	2		T
G17	PR13B	2		C	G17	PR15B	2		C
GND	GNDIO	2			GND	GNDIO	2		
E20	PR12B	2		C*	E20	PR14B	2		C*
F19	PR13A	2		T	F19	PR15A	2		T
D20	PR12A	2		T*	D20	PR14A	2		T*
F18	PR11B	2		C	F18	PR13B	2		C
C21	PR10B	2		C*	C21	PR12B	2		C*
F16	PR11A	2		T	F16	PR13A	2		T
C22	PR10A	2		T*	C22	PR12A	2		T*
GND	GNDIO	2			GND	GNDIO	2		
D19	PR2B	2	VREF2_2	C*	D19	PR2B	2	VREF2_2	C*
E19	PR2A	2	VREF1_2	T*	E19	PR2A	2	VREF1_2	T*
B21	PT73B	1	VREF2_1	C	B21	PT82B	1	VREF2_1	C
B22	PT73A	1	VREF1_1	T	B22	PT82A	1	VREF1_1	T
GND	GNDIO	1			GND	GNDIO	1		
D18	PT71B	1		C	D18	PT80B	1		C
C20	PT72B	1		C	C20	PT81B	1		C
E18	PT71A	1		T	E18	PT80A	1		T
C19	PT72A	1		T	C19	PT81A	1		T
B20	PT70B	1		C	B20	PT79B	1		C
D17	PT69B	1		C	D17	PT78B	1		C
C18	PT69A	1		T	C18	PT78A	1		T
GND	GNDIO	1			GND	GNDIO	1		
A19	PT70A	1		T	A19	PT79A	1		T
A18	PT67B	1		C	A18	PT76B	1		C
A21	PT68B	1		C	A21	PT77B	1		C
B18	PT67A	1		T	B18	PT76A	1		T
A20	PT68A	1		T	A20	PT77A	1		T
D16	PT65B	1		C	D16	PT74B	1		C
G16	PT66B	1		C	G16	PT75B	1		C
E16	PT65A	1		T	E16	PT74A	1		T
G15	PT66A	1		T	G15	PT75A	1		T
C17	PT55B	1		C	C17	PT64B	1		C

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	1			GND	GNDIO	1		
C16	PT55A	1		T	C16	PT64A	1		T
A17	PT53B	1		C	A17	PT62B	1		C
B17	PT54B	1		C	B17	PT63B	1		C
A16	PT53A	1		T	A16	PT62A	1		T
B16	PT54A	1		T	B16	PT63A	1		T
E15	PT51B	1		C	E15	PT60B	1		C
C15	PT52B	1		C	C15	PT61B	1		C
F15	PT51A	1		T	F15	PT60A	1		T
GND	GNDIO	1			GND	GNDIO	1		
D15	PT52A	1		T	D15	PT61A	1		T
B15	PT49B	1		C	B15	PT58B	1		C
A15	PT49A	1		T	A15	PT58A	1		T
A14	PT48A	1		T	A14	PT57A	1		T
B14	PT48B	1		C	B14	PT57B	1		C
D14	PT46B	1		C	D14	PT55B	1		C
E14	PT45B	1		C	E14	PT54B	1		C
C13	PT46A	1		T	C13	PT55A	1		T
GND	GNDIO	1			GND	GNDIO	1		
F14	PT45A	1		T	F14	PT54A	1		T
A13	PT44B	1		C	A13	PT53B	1		C
E13	PT43B	1		C	E13	PT52B	1		C
B13	PT44A	1		T	B13	PT53A	1		T
D13	PT43A	1		T	D13	PT52A	1		T
E12	PT42B	1		C	E12	PT51B	1		C
D12	PT42A	1		T	D12	PT51A	1		T
GND	GNDIO	1			GND	GNDIO	1		
A12	PT40B	1		C	A12	PT49B	1		C
B12	PT39B	1	PCLKC1_0	C	B12	PT48B	1	PCLKC1_0	C
A11	PT40A	1		T	A11	PT49A	1		T
C12	PT39A	1	PCLKT1_0	T	C12	PT48A	1	PCLKT1_0	T
F12	XRES	1			F12	XRES	1		
GND	GNDIO	0			GND	GNDIO	0		
B10	PT37B	0	PCLKC0_0	C	B10	PT46B	0	PCLKC0_0	C
B11	PT37A	0	PCLKT0_0	T	B11	PT46A	0	PCLKT0_0	T
C11	PT35B	0		C	C11	PT44B	0		C
A10	PT36B	0		C	A10	PT45B	0		C
C10	PT35A	0		T	C10	PT44A	0		T
A9	PT36A	0		T	A9	PT45A	0		T
A8	PT33B	0		C	A8	PT42B	0		C
E11	PT34B	0		C	E11	PT43B	0		C
A7	PT33A	0		T	A7	PT42A	0		T
F11	PT34A	0		T	F11	PT43A	0		T
B8	PT32B	0		C	B8	PT41B	0		C

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	0			GND	GNDIO	0		
B9	PT32A	0		T	B9	PT41A	0		T
C8	PT29B	0		C	C8	PT38B	0		C
B7	PT30B	0		C	B7	PT39B	0		C
D8	PT29A	0		T	D8	PT38A	0		T
GND	GNDIO	0			GND	GNDIO	0		
A6	PT30A	0		T	A6	PT39A	0		T
C7	PT26B	0		C	C7	PT35B	0		C
D10	PT27B	0		C	D10	PT36B	0		C
C6	PT26A	0		T	C6	PT35A	0		T
E10	PT27A	0		T	E10	PT36A	0		T
F10	PT24B	0		C	F10	PT33B	0		C
B6	PT25B	0		C	B6	PT34B	0		C
D9	PT24A	0		T	D9	PT33A	0		T
B5	PT25A	0		T	B5	PT34A	0		T
GND	GNDIO	0			GND	GNDIO	0		
A5	PT22B	0		C	A5	PT31B	0		C
F9	PT23B	0		C	F9	PT32B	0		C
A4	PT22A	0		T	A4	PT31A	0		T
E9	PT23A	0		T	E9	PT32A	0		T
G8	PT20B	0		C	G8	PT29B	0		C
A3	PT21B	0		C	A3	PT30B	0		C
E8	PT20A	0		T	E8	PT29A	0		T
A2	PT21A	0		T	A2	PT30A	0		T
C3	PT10B	0		C	C3	PT10B	0		C
GND	GNDIO	0			GND	GNDIO	0		
B3	PT10A	0		T	B3	PT10A	0		T
E7	PT8B	0		C	E7	PT8B	0		C
F8	PT9B	0		C	F8	PT9B	0		C
F7	PT8A	0		T	F7	PT8A	0		T
D7	PT9A	0		T	D7	PT9A	0		T
D4	PT6B	0		C	D4	PT6B	0		C
D5	PT7B	0		C	D5	PT7B	0		C
C4	PT6A	0		T	C4	PT6A	0		T
D6	PT7A	0		T	D6	PT7A	0		T
J7	PT4B	0		C	J7	PT4B	0		C
B2	PT5B	0		C	B2	PT5B	0		C
GND	GNDIO	0			GND	GNDIO	0		
H7	PT4A	0		T	H7	PT4A	0		T
B1	PT5A	0		T	B1	PT5A	0		T
D1	PT2B	0	VREF2_0	C	D1	PT2B	0	VREF2_0	C
D3	PT3B	0		C	D3	PT3B	0		C
C1	PT2A	0	VREF1_0	T	C1	PT2A	0	VREF1_0	T
C2	PT3A	0		T	C2	PT3A	0		T

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J10	VCC	-			J10	VCC	-		
J11	VCC	-			J11	VCC	-		
J12	VCC	-			J12	VCC	-		
J13	VCC	-			J13	VCC	-		
K14	VCC	-			K14	VCC	-		
K9	VCC	-			K9	VCC	-		
L14	VCC	-			L14	VCC	-		
L9	VCC	-			L9	VCC	-		
M14	VCC	-			M14	VCC	-		
M9	VCC	-			M9	VCC	-		
N14	VCC	-			N14	VCC	-		
N9	VCC	-			N9	VCC	-		
P10	VCC	-			P10	VCC	-		
P11	VCC	-			P11	VCC	-		
P12	VCC	-			P12	VCC	-		
P13	VCC	-			P13	VCC	-		
G10	VCCIO0	0			G10	VCCIO0	0		
G9	VCCIO0	0			G9	VCCIO0	0		
H8	VCCIO0	0			H8	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0		
G11	VCCIO1	1			G11	VCCIO1	1		
G12	VCCIO1	1			G12	VCCIO1	1		
G13	VCCIO1	1			G13	VCCIO1	1		
G14	VCCIO1	1			G14	VCCIO1	1		
H14	VCCIO2	2			H14	VCCIO2	2		
H15	VCCIO2	2			H15	VCCIO2	2		
J15	VCCIO2	2			J15	VCCIO2	2		
K16	VCCIO2	2			K16	VCCIO2	2		
L16	VCCIO3	3			L16	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3		
N16	VCCIO3	3			N16	VCCIO3	3		
P16	VCCIO3	3			P16	VCCIO3	3		
R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4		
T13	VCCIO4	4			T13	VCCIO4	4		
T14	VCCIO4	4			T14	VCCIO4	4		
R9	VCCIO5	5			R9	VCCIO5	5		
T10	VCCIO5	5			T10	VCCIO5	5		
T11	VCCIO5	5			T11	VCCIO5	5		
T9	VCCIO5	5			T9	VCCIO5	5		
N7	VCCIO6	6			N7	VCCIO6	6		
P7	VCCIO6	6			P7	VCCIO6	6		
P8	VCCIO6	6			P8	VCCIO6	6		
R8	VCCIO6	6			R8	VCCIO6	6		

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J8	VCCIO7	7			J8	VCCIO7	7		
K7	VCCIO7	7			K7	VCCIO7	7		
L7	VCCIO7	7			L7	VCCIO7	7		
M7	VCCIO7	7			M7	VCCIO7	7		
P15	VCCIO8	8			P15	VCCIO8	8		
R15	VCCIO8	8			R15	VCCIO8	8		
C5	VCCAUX	-			C5	VCCAUX	-		
D11	VCCAUX	-			D11	VCCAUX	-		
E17	VCCAUX	-			E17	VCCAUX	-		
E6	VCCAUX	-			E6	VCCAUX	-		
F13	VCCAUX	-			F13	VCCAUX	-		
G18	VCCAUX	-			G18	VCCAUX	-		
G5	VCCAUX	-			G5	VCCAUX	-		
K5	VCCAUX	-			K5	VCCAUX	-		
M17	VCCAUX	-			M17	VCCAUX	-		
P17	VCCAUX	-			P17	VCCAUX	-		
R5	VCCAUX	-			R5	VCCAUX	-		
V11	VCCAUX	-			V11	VCCAUX	-		
V13	VCCAUX	-			V13	VCCAUX	-		
V15	VCCAUX	-			V15	VCCAUX	-		
V7	VCCAUX	-			V7	VCCAUX	-		
V8	VCCAUX	-			V8	VCCAUX	-		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		
AA19	GND	-			AA19	GND	-		
AA4	GND	-			AA4	GND	-		
AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-		
B19	GND	-			B19	GND	-		
B4	GND	-			B4	GND	-		
C14	GND	-			C14	GND	-		
C9	GND	-			C9	GND	-		
D2	GND	-			D2	GND	-		
D21	GND	-			D21	GND	-		
F17	GND	-			F17	GND	-		
F6	GND	-			F6	GND	-		
H10	GND	-			H10	GND	-		
H11	GND	-			H11	GND	-		
H12	GND	-			H12	GND	-		
H13	GND	-			H13	GND	-		
J14	GND	-			J14	GND	-		
J20	GND	-			J20	GND	-		
J3	GND	-			J3	GND	-		
J9	GND	-			J9	GND	-		

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-		
K15	GND	-			K15	GND	-		
K8	GND	-			K8	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-		
L15	GND	-			L15	GND	-		
L8	GND	-			L8	GND	-		
M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-		
M15	GND	-			M15	GND	-		
M8	GND	-			M8	GND	-		
N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N15	GND	-			N15	GND	-		
N8	GND	-			N8	GND	-		
P14	GND	-			P14	GND	-		
P20	GND	-			P20	GND	-		
P3	GND	-			P3	GND	-		
P9	GND	-			P9	GND	-		
R10	GND	-			R10	GND	-		
R11	GND	-			R11	GND	-		
R12	GND	-			R12	GND	-		
R13	GND	-			R13	GND	-		
U17	GND	-			U17	GND	-		
U6	GND	-			U6	GND	-		
W2	GND	-			W2	GND	-		
W21	GND	-			W21	GND	-		
Y14	GND	-			Y14	GND	-		
Y9	GND	-			Y9	GND	-		
H6	NC	-			H6	PL25A	7	LUM0_SPLLT_IN_A	T
J6	NC	-			J6	PL25B	7	LUM0_SPLLC_IN_A	C
H3	NC	-			H3	PL26A	7	LUM0_SPLLT_FB_A	T
H2	NC	-			H2	PL26B	7	LUM0_SPLLC_FB_A	C
H17	NC	-			H17	PR26B	2	RUM0_SPLLC_FB_A	C
H16	NC	-			H16	PR26A	2	RUM0_SPLLT_FB_A	T

LFE2-35E/35SE and LFE2-50E/50SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/35SE					LFE2-50E/50SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
H20	NC	-			H20	PR25B	2	RUM0_SPLLC_IN_A	C
H18	NC	-			H18	PR25A	2	RUM0_SPLLT_IN_A	T

* Supports true LVDS outputs.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D2	PL2A	7	VREF2_7	T*	D2	PL2A	7	VREF2_7	T*
D1	PL2B	7	VREF1_7	C*	D1	PL2B	7	VREF1_7	C*
GND	GNDIO7	7			GNDIO	GNDIO7	7		
F6	PL3A	7		T	F6	PL3A	7		T
F5	PL3B	7		C	F5	PL3B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
E4	NC	-			E4	PL4A	7		T*
E3	NC	-			E3	PL4B	7		C*
E2	NC	-			E2	PL5A	7		T
E1	NC	-			E1	PL5B	7		C
GND	GNDIO7	7			GNDIO	GNDIO7	7		
H6	NC	-			H6	PL6A	7	LDQS6	T*
H5	NC	-			H5	PL6B	7		C*
F2	NC	-			F2	PL7A	7		T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
F1	NC	-			F1	PL7B	7		C
H8	NC	-			H8	PL8A	7		T*
J9	NC	-			J9	PL8B	7		C*
G4	NC	-			G4	PL9A	7		T
GND	GNDIO7	7			GNDIO	GNDIO7	7		
G3	NC	-			G3	PL9B	7		C
H7	PL4A	7		T*	H7	PL10A	7		T*
J8	PL4B	7		C*	J8	PL10B	7		C*
G2	PL5A	7		T	G2	PL11A	7		T
G1	PL5B	7		C	G1	PL11B	7		C
H3	PL6A	7		T*	H3	PL12A	7		T*
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
H4	PL6B	7		C*	H4	PL12B	7		C*
J5	PL7A	7		T	J5	PL13A	7		T
J4	PL7B	7		C	J4	PL13B	7		C
J3	PL8A	7	LDQS8	T*	J3	PL14A	7	LDQS14	T*
GND	GNDIO7	7			GNDIO	GNDIO7	7		
K4	PL8B	7		C*	K4	PL14B	7		C*
H1	PL9A	7		T	H1	PL15A	7		T
H2	PL9B	7		C	H2	PL15B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
K6	PL10A	7		T*	K6	PL16A	7		T*
K7	PL10B	7		C*	K7	PL16B	7		C*
J1	PL11A	7		T	J1	PL17A	7		T
J2	PL11B	7		C	J2	PL17B	7		C
GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
K3	NC	-			K3	NC	-		
K2	NC	-			K2	NC	-		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO7	7			GND	GNDIO7	7		
K1	NC	-			K1	NC	-		
L2	NC	-			L2	NC	-		
L1	NC	-			L1	NC	-		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
M2	NC	-			M2	NC	-		
M1	NC	-			M1	NC	-		
N2	NC	-			N2	NC	-		
GND	GNDIO7	7			GND	GNDIO7	7		
M8	VCC	-			M8	NC	-		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
GND	GNDIO7	7			GND	GNDIO7	7		
N1	PL12A	7			N1	PL18A	7		
L8	PL13A	7		T	L8	PL19A	7		T
K8	PL13B	7		C	K8	PL19B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
L6	PL14A	7		T*	L6	PL20A	7		T*
K5	PL14B	7		C*	K5	PL20B	7		C*
L7	PL15A	7		T	L7	PL21A	7		T
L5	PL15B	7		C	L5	PL21B	7		C
GND	GNDIO7	7			GND	GNDIO7	7		
P1	PL16A	7	LDQS16	T*	P1	PL22A	7	LDQS22	T*
P2	PL16B	7		C*	P2	PL22B	7		C*
M6	PL17A	7		T	M6	PL23A	7		T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
N8	PL17B	7		C	N8	PL23B	7		C
R1	PL18A	7		T*	R1	PL24A	7		T*
R2	PL18B	7		C*	R2	PL24B	7		C*
M7	PL19A	7	PCLKT7_0	T	M7	PL25A	7	PCLKT7_0	T
GND	GNDIO7	7			GND	GNDIO7	7		
N9	PL19B	7	PCLKC7_0	C	N9	PL25B	7	PCLKC7_0	C
M4	PL21A	6	PCLKT6_0	T*	M4	PL27A	6	PCLKT6_0	T*
M5	PL21B	6	PCLKC6_0	C*	M5	PL27B	6	PCLKC6_0	C*
N7	PL22A	6	VREF2_6	T	N7	PL28A	6	VREF2_6	T
P9	PL22B	6	VREF1_6	C	P9	PL28B	6	VREF1_6	C
N3	PL23A	6		T*	N3	PL29A	6		T*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
N4	PL23B	6		C*	N4	PL29B	6		C*
N5	PL24A	6		T	N5	PL30A	6		T
P7	PL24B	6		C	P7	PL30B	6		C
T1	NC	-			T1	PL31A	6	LDQS31	T*
GND	GNDIO6	6			GNDIO	GNDIO6	6		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
T2	NC	-			T2	PL31B	6		C*
P8	NC	-			P8	PL32A	6		T
P6	NC	-			P6	PL32B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
P5	NC	-			P5	PL33A	6		T*
P4	NC	-			P4	PL33B	6		C*
U1	NC	-			U1	PL34A	6		T
V1	NC	-			V1	PL34B	6		C
GND	GNDIO6	6			GNDIO	GNDIO6	6		
P3	NC	-			P3	NC	-		
R3	NC	-			R3	NC	-		
R4	NC	-			R4	NC	-		
U2	NC	-			U2	NC	-		
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
V2	NC	-			V2	NC	-		
W2	NC	-			W2	NC	-		
T6	NC	-			T6	PL38A	6		T
R5	NC	-			R5	PL38B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
R6	PL25A	6	LDQS25	T*	R6	PL39A	6	LDQS39	T*
R7	PL25B	6		C*	R7	PL39B	6		C*
W1	PL26A	6		T	W1	PL40A	6		T
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
Y2	PL26B	6		C	Y2	PL40B	6		C
Y1	PL27A	6	LLM0_GDLLT_IN_A**	T*	Y1	PL41A	6	LLM0_GDLLT_IN_A**	T*
AA2	PL27B	6	LLM0_GDLLC_IN_A**	C*	AA2	PL41B	6	LLM0_GDLLC_IN_A**	C*
T5	PL28A	6	LLM0_GDLLT_FB_A	T	T5	PL42A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO6	6			GND	GNDIO6	6		
T7	PL28B	6	LLM0_GDLLC_FB_A	C	T7	PL42B	6	LLM0_GDLLC_FB_A	C
R8	VCC	6			R8	VCCPLL	6		
T8	LLM0_PLLCAP	6			T8	LLM0_PLLCAP	6		
U3	PL30A	6	LLM0_GPLLT_IN_A**	T*	U3	PL44A	6	LLM0_GPLLT_IN_A**	T*
U4	PL30B	6	LLM0_GPLLC_IN_A**	C*	U4	PL44B	6	LLM0_GPLLC_IN_A**	C*
V3	PL31A	6	LLM0_GPLLT_FB_A	T	V3	PL45A	6	LLM0_GPLLT_FB_A	T
U5	PL31B	6	LLM0_GPLLC_FB_A	C	U5	PL45B	6	LLM0_GPLLC_FB_A	C
V4	PL32A	6		T*	V4	PL46A	6		T*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
V5	PL32B	6		C*	V5	PL46B	6		C*
Y3	PL33A	6		T	Y3	PL47A	6		T
Y4	PL33B	6		C	Y4	PL47B	6		C
W3	PL34A	6	LDQS34	T*	W3	PL48A	6	LDQS48	T*
GND	GNDIO6	6			GND	GNDIO6	6		
W4	PL34B	6		C*	W4	PL48B	6		C*
AA1	PL35A	6		T	AA1	PL49A	6		T

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AB1	PL35B	6		C	AB1	PL49B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
U8	PL36A	6		T*	U8	PL50A	6		T*
U7	PL36B	6		C*	U7	PL50B	6		C*
V8	PL37A	6		T	V8	PL51A	6		T
U6	PL37B	6		C	U6	PL51B	6		C
GND	GNDIO6	6			GNDIO	GNDIO6	6		
W6	PL38A	6		T*	W6	PL52A	6		T*
W5	PL38B	6		C*	W5	PL52B	6		C*
AC1	PL39A	6		T	AC1	PL53A	6		T
AD1	PL39B	6		C	AD1	PL53B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
Y6	PL40A	6		T*	Y6	PL54A	6		T*
Y5	PL40B	6		C*	Y5	PL54B	6		C*
AE2	PL41A	6		T	AE2	PL55A	6		T
AD2	PL41B	6		C	AD2	PL55B	6		C
GND	GNDIO6	6			GNDIO	GNDIO6	6		
AB3	PL42A	6	LDQS42	T*	AB3	PL56A	6	LDQS56	T*
AB2	PL42B	6		C*	AB2	PL56B	6		C*
W7	PL43A	6		T	W7	PL57A	6		T
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
W8	PL43B	6		C	W8	PL57B	6		C
Y7	PL44A	6		T*	Y7	PL58A	6		T*
Y8	PL44B	6		C*	Y8	PL58B	6		C*
AC2	PL45A	6		T	AC2	PL59A	6		T
GND	GNDIO6	6			GNDIO	GNDIO6	6		
AD3	PL45B	6		C	AD3	PL59B	6		C
AC3	TCK	-			AC3	TCK	-		
AA8	TDI	-			AA8	TDI	-		
AB4	TMS	-			AB4	TMS	-		
AA5	TDO	-			AA5	TDO	-		
AB5	VCCJ	-			AB5	VCCJ	-		
AE3	PB2A	5	VREF2_5	T	AE3	PB2A	5	VREF2_5	T
AF3	PB2B	5	VREF1_5	C	AF3	PB2B	5	VREF1_5	C
AC4	PB3A	5		T	AC4	PB3A	5		T
AD4	PB3B	5		C	AD4	PB3B	5		C
AE4	PB4A	5		T	AE4	PB4A	5		T
AF4	PB4B	5		C	AF4	PB4B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
V9	PB5A	5		T	V9	PB5A	5		T
W9	PB5B	5		C	W9	PB5B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AA6	PB6A	5	BDQS6	T	AA6	PB6A	5	BDQS6	T
AB6	PB6B	5		C	AB6	PB6B	5		C

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AC5	PB7A	5		T	AC5	PB7A	5		T
AD5	PB7B	5		C	AD5	PB7B	5		C
AA7	PB8A	5		T	AA7	PB8A	5		T
AB7	PB8B	5		C	AB7	PB8B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AE5	PB9A	5		T	AE5	PB9A	5		T
AF5	PB9B	5		C	AF5	PB9B	5		C
AC7	PB10A	5		T	AC7	PB10A	5		T
AD7	PB10B	5		C	AD7	PB10B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
W10	PB11A	5		T	W10	PB11A	5		T
Y10	PB11B	5		C	Y10	PB11B	5		C
W11	PB12A	5		T	W11	PB12A	5		T
AA10	PB12B	5		C	AA10	PB12B	5		C
AC8	PB13A	5		T	AC8	PB13A	5		T
AD8	PB13B	5		C	AD8	PB13B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AB8	PB14A	5		T	AB8	PB14A	5		T
AB10	PB14B	5		C	AB10	PB14B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AE6	PB15A	5	BDQS15	T	AE6	PB15A	5	BDQS15	T
AF6	PB15B	5		C	AF6	PB15B	5		C
AA11	PB16A	5		T	AA11	PB16A	5		T
AC9	PB16B	5		C	AC9	PB16B	5		C
AB9	PB17A	5		T	AB9	PB17A	5		T
AD9	PB17B	5		C	AD9	PB17B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y11	PB18A	5		T	Y11	PB18A	5		T
AB11	PB18B	5		C	AB11	PB18B	5		C
AE7	PB19A	5		T	AE7	PB19A	5		T
AF7	PB19B	5		C	AF7	PB19B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AC10	PB20A	5		T	AC10	PB20A	5		T
AD10	PB20B	5		C	AD10	PB20B	5		C
AA12	PB21A	5		T	AA12	PB21A	5		T
W12	PB21B	5		C	W12	PB21B	5		C
AB12	PB22A	5		T	AB12	PB22A	5		T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y12	PB22B	5		C	Y12	PB22B	5		C
AD12	PB23A	5		T	AD12	PB23A	5		T

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AC12	PB23B	5		C	AC12	PB23B	5		C
AC13	PB24A	5	BDQS24	T	AC13	PB24A	5	BDQS24	T
GND	GNDIO5	5			GND	GNDIO5	5		
AA13	PB24B	5		C	AA13	PB24B	5		C
AD13	PB25A	5		T	AD13	PB25A	5		T
AC14	PB25B	5		C	AC14	PB25B	5		C
AE8	PB26A	5		T	AE8	PB26A	5		T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AF8	PB26B	5		C	AF8	PB26B	5		C
AB15	PB27A	5		T	AB15	PB27A	5		T
Y13	PB27B	5		C	Y13	PB27B	5		C
AE9	PB28A	5		T	AE9	PB28A	5		T
GND	GNDIO5	5			GND	GNDIO5	5		
AF9	PB28B	5		C	AF9	PB28B	5		C
W13	PB29A	5		T	W13	PB29A	5		T
AA14	PB29B	5		C	AA14	PB29B	5		C
AE10	PB30A	5		T	AE10	PB30A	5		T
AF10	PB30B	5		C	AF10	PB30B	5		C
W14	PB31A	5		T	W14	PB31A	5		T
AB13	PB31B	5		C	AB13	PB31B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y14	PB32A	5		T	Y14	PB32A	5		T
AB14	PB32B	5		C	AB14	PB32B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AE11	PB33A	5	BDQS33	T	AE11	PB33A	5	BDQS33	T
AF11	PB33B	5		C	AF11	PB33B	5		C
AD14	PB34A	5		T	AD14	PB34A	5		T
AA15	PB34B	5		C	AA15	PB34B	5		C
AE12	PB35A	5	PCLKT5_0	T	AE12	PB35A	5	PCLKT5_0	T
AF12	PB35B	5	PCLKC5_0	C	AF12	PB35B	5	PCLKC5_0	C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
AD15	PB40A	4	PCLKT4_0	T	AD15	PB40A	4	PCLKT4_0	T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AC15	PB40B	4	PCLKC4_0	C	AC15	PB40B	4	PCLKC4_0	C
AE13	PB41A	4		T	AE13	PB41A	4		T
AF13	PB41B	4		C	AF13	PB41B	4		C
AB17	PB42A	4	BDQS42	T	AB17	PB42A	4	BDQS42	T
GND	GNDIO4	4			GND	GNDIO4	4		
Y15	PB42B	4		C	Y15	PB42B	4		C
AE14	PB43A	4		T	AE14	PB43A	4		T
AF14	PB43B	4		C	AF14	PB43B	4		C
AA16	PB44A	4		T	AA16	PB44A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
W15	PB44B	4		C	W15	PB44B	4		C
AC17	PB45A	4		T	AC17	PB45A	4		T
AB16	PB45B	4		C	AB16	PB45B	4		C
AE15	PB46A	4		T	AE15	PB46A	4		T
GND	GNDIO4	4			GND	GNDIO4	4		
AF15	PB46B	4		C	AF15	PB46B	4		C
AE16	PB47A	4		T	AE16	PB47A	4		T
AF16	PB47B	4		C	AF16	PB47B	4		C
Y16	PB48A	4		T	Y16	PB48A	4		T
AB18	PB48B	4		C	AB18	PB48B	4		C
AD17	PB49A	4		T	AD17	PB49A	4		T
AD18	PB49B	4		C	AD18	PB49B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AC18	PB50A	4		T	AC18	PB50A	4		T
AD19	PB50B	4		C	AD19	PB50B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AC19	PB51A	4	BDQS51	T	AC19	PB51A	4	BDQS51	T
AE17	PB51B	4		C	AE17	PB51B	4		C
AB19	PB52A	4		T	AB19	PB52A	4		T
AE19	PB52B	4		C	AE19	PB52B	4		C
AF17	PB53A	4		T	AF17	PB53A	4		T
AE18	PB53B	4		C	AE18	PB53B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
W16	PB54A	4		T	W16	PB54A	4		T
AA17	PB54B	4		C	AA17	PB54B	4		C
AF18	PB55A	4		T	AF18	PB55A	4		T
AF19	PB55B	4		C	AF19	PB55B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AA19	NC	-			AA19	PB56A	4		T
W17	NC	-			W17	PB56B	4		C
Y19	NC	-			Y19	PB57A	4		T
Y17	NC	-			Y17	PB57B	4		C
AF20	NC	-			AF20	NC	-		
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AE20	NC	-			AE20	NC	-		
AA20	NC	-			AA20	NC	-		
W18	NC	-			W18	NC	-		
AD20	NC	-			AD20	NC	-		
GND	GNDIO4	4			GND	GNDIO4	4		
AE21	NC	-			AE21	NC	-		
AF21	NC	-			AF21	NC	-		
AF22	NC	-			AF22	NC	-		
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
GND	GNDIO4	4			GND	GNDIO4	4		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AE22	PB56A	4		T	AE22	PB65A	4		T
AD22	PB56B	4		C	AD22	PB65B	4		C
AF23	PB57A	4		T	AF23	PB66A	4		T
AE23	PB57B	4		C	AE23	PB66B	4		C
AD23	PB58A	4		T	AD23	PB67A	4		T
AC23	PB58B	4		C	AC23	PB67B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AB20	PB59A	4		T	AB20	PB68A	4		T
AC20	PB59B	4		C	AC20	PB68B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AB21	PB60A	4	BDQS60	T	AB21	PB69A	4	BDQS69	T
AC22	PB60B	4		C	AC22	PB69B	4		C
W19	PB61A	4		T	W19	PB70A	4		T
AA21	PB61B	4		C	AA21	PB70B	4		C
AF24	PB62A	4		T	AF24	PB71A	4		T
AE24	PB62B	4		C	AE24	PB71B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
Y20	PB63A	4		T	Y20	PB72A	4		T
AB22	PB63B	4		C	AB22	PB72B	4		C
Y21	PB64A	4	VREF2_4	T	Y21	PB73A	4	VREF2_4	T
AB23	PB64B	4	VREF1_4	C	AB23	PB73B	4	VREF1_4	C
GND	GNDIO4	4			GND	GNDIO4	4		
AD24	CFG2	8			AD24	CFG2	8		
W20	CFG1	8			W20	CFG1	8		
AC24	CFG0	8			AC24	CFG0	8		
V19	PROGRAMN	8			V19	PROGRAMN	8		
AA22	CCLK	8			AA22	CCLK	8		
AB24	INITN	8			AB24	INITN	8		
AD25	DONE	8			AD25	DONE	8		
GND	GNDIO8	8			GND	GNDIO	8		
W21	PR44B	8	WRITEN	C	W21	PR58B	8	WRITEN	C
Y22	PR44A	8	CS1N	T	Y22	PR58A	8	CS1N	T
AC25	PR43B	8	CSN	C	AC25	PR57B	8	CSN	C
AB25	PR43A	8	D0	T	AB25	PR57A	8	D0	T
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		
AD26	PR42B	8	D1	C	AD26	PR56B	8	D1	C
AC26	PR42A	8	D2	T	AC26	PR56A	8	D2	T
Y23	PR41B	8	D3	C	Y23	PR55B	8	D3	C
GND	GNDIO8	8			GND	GNDIO	8		
W22	PR41A	8	D4	T	W22	PR55A	8	D4	T
AA25	PR40B	8	D5	C	AA25	PR54B	8	D5	C
AB26	PR40A	8	D6	T	AB26	PR54A	8	D6	T
W23	PR39B	8	D7	C	W23	PR53B	8	D7	C
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
V22	PR39A	8	DI	T	V22	PR53A	8	DI	T
Y24	PR38B	8	DOUT,CSON	C	Y24	PR52B	8	DOUT_CSON	C
Y25	PR38A	8	BUSY	T	Y25	PR52A	8	BUSY	T
W24	PR37B	3		C	W24	PR51B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
V23	PR37A	3		T	V23	PR51A	3		T
AA26	PR36B	3		C*	AA26	PR50B	3		C*
Y26	PR36A	3		T*	Y26	PR50A	3		T*
U21	PR35B	3		C	U21	PR49B	3		C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
U19	PR35A	3		T	U19	PR49A	3		T
W25	PR34B	3		C*	W25	PR48B	3		C*
W26	PR34A	3	RDQS34	T*	W26	PR48A	3	RDQS48	T*
GND	GNDIO3	3			GND	GNDIO3	3		
V24	PR33B	3		C	V24	PR47B	3		C
V25	PR33A	3		T	V25	PR47A	3		T
V26	PR32B	3		C*	V26	PR46B	3		C*
U26	PR32A	3		T*	U26	PR46A	3		T*
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
U22	PR31B	3	RLM0_GPLLC_FB_A	C	U22	PR45B	3	RLM0_GPLLC_FB_A	C
U23	PR31A	3	RLM0_GPLLT_FB_A	T	U23	PR45A	3	RLM0_GPLLT_FB_A	T
U24	PR30B	3	RLM0_GPLLC_IN_A**	C*	U24	PR44B	3	RLM0_GPLLC_IN_A**	C*
U25	PR30A	3	RLM0_GPLLT_IN_A**	T*	U25	PR44A	3	RLM0_GPLLT_IN_A**	T*
R20	RLM0_PLLCAP	3			R20	RLM0_PLLCAP	3		
P18	VCC	3			P18	VCCPLL	3		
T19	PR28B	3	RLM0_GDLLC_FB_A	C	T19	PR42B	3	RLM0_GDLLC_FB_A	C
U20	PR28A	3	RLM0_GDLLT_FB_A	T	U20	PR42A	3	RLM0_GDLLT_FB_A	T
GND	GNDIO3	3			GND	GNDIO3	3		
T25	PR27B	3	RLM0_GDLLC_IN_A**	C*	T25	PR41B	3	RLM0_GDLLC_IN_A**	C*
T26	PR27A	3	RLM0_GDLLT_IN_A**	T*	T26	PR41A	3	RLM0_GDLLT_IN_A**	T*
T20	PR26B	3		C	T20	PR40B	3		C
T22	PR26A	3		T	T22	PR40A	3		T
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R26	PR25B	3		C*	R26	PR39B	3		C*
R25	PR25A	3	RDQS25	T*	R25	PR39A	3	RDQS39	T*
R22	NC	-			R22	PR38B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
T21	NC	-			T21	PR38A	3		T
P26	NC	-			P26	NC	-		
P25	NC	-			P25	NC	-		
R24	NC	-			R24	NC	-		
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R23	NC	-			R23	NC	-		
P20	NC	-			P20	NC	-		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
R19	NC	-			R19	NC	-		
P21	NC	-			P21	PR34B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
P19	NC	-			P19	PR34A	3		T
P23	NC	-			P23	PR33B	3		C*
P22	NC	-			P22	PR33A	3		T*
N22	NC	-			N22	PR32B	3		C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R21	NC	-			R21	PR32A	3		T
N26	NC	-			N26	PR31B	3		C*
N25	NC	-			N25	PR31A	3	RDQS31	T*
GND	GNDIO3	3			GND	GNDIO3	3		
N19	PR24B	3		C	N19	PR30B	3		C
N20	PR24A	3		T	N20	PR30A	3		T
M26	PR23B	3		C*	M26	PR29B	3		C*
M25	PR23A	3		T*	M25	PR29A	3		T*
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
N18	PR22B	3	VREF2_3	C	N18	PR28B	3	VREF2_3	C
N21	PR22A	3	VREF1_3	T	N21	PR28A	3	VREF1_3	T
L26	PR21B	3	PCLKC3_0	C*	L26	PR27B	3	PCLKC3_0	C*
L25	PR21A	3	PCLKT3_0	T*	L25	PR27A	3	PCLKT3_0	T*
N24	PR19B	2	PCLKC2_0	C	N24	PR25B	2	PCLKC2_0	C
M23	PR19A	2	PCLKT2_0	T	M23	PR25A	2	PCLKT2_0	T
GND	GNDIO2	2			GND	GNDIO2	2		
L21	PR18B	2		C*	L21	PR24B	2		C*
K22	PR18A	2		T*	K22	PR24A	2		T*
M24	PR17B	2		C	M24	PR23B	2		C
N23	PR17A	2		T	N23	PR23A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
K26	PR16B	2		C*	K26	PR22B	2		C*
K25	PR16A	2	RDQS16	T*	K25	PR22A	2	RDQS22	T*
M20	PR15B	2		C	M20	PR21B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
M19	PR15A	2		T	M19	PR21A	2		T
L22	PR14B	2		C*	L22	PR20B	2		C*
M22	PR14A	2		T*	M22	PR20A	2		T*
K21	PR13B	2		C	K21	PR19B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
M21	PR13A	2		T	M21	PR19A	2		T
K24	PR12B	2		C*	K24	PR18B	2		C*
J24	PR12A	2		T*	J24	PR18A	2		T*
GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
GND	GNDIO2	2			GND	GNDIO2	2		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
L20	VCC	-			L20	NC	-		
GND	GNDIO2	2			GND	GNDIO2	2		
J26	NC	-			J26	NC	-		
J25	NC	-			J25	NC	-		
J23	NC	-			J23	NC	-		
K23	NC	-			K23	NC	-		
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H26	NC	-			H26	NC	-		
H25	NC	-			H25	NC	-		
H24	NC	-			H24	NC	-		
GND	GNDIO2	2			GND	GNDIO2	2		
H23	NC	-			H23	NC	-		
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
G26	PR11B	2		C	G26	PR17B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
G25	PR11A	2		T	G25	PR17A	2		T
F26	PR10B	2		C*	F26	PR16B	2		C*
F25	PR10A	2		T*	F25	PR16A	2		T*
K20	PR9B	2		C	K20	PR15B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
L19	PR9A	2		T	L19	PR15A	2		T
E26	PR8B	2		C*	E26	PR14B	2		C*
E25	PR8A	2	RDQS8	T*	E25	PR14A	2	RDQS14	T*
GND	GNDIO2	2			GND	GNDIO2	2		
J22	PR7B	2		C	J22	PR13B	2		C
H22	PR7A	2		T	H22	PR13A	2		T
G24	PR6B	2		C*	G24	PR12B	2		C*
G23	PR6A	2		T*	G23	PR12A	2		T*
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
K19	PR5B	2		C	K19	PR11B	2		C
J19	PR5A	2		T	J19	PR11A	2		T
D26	PR4B	2		C*	D26	PR10B	2		C*
C26	PR4A	2		T*	C26	PR10A	2		T*
F22	NC	-			F22	PR9B	2		C
E24	NC	-			E24	PR9A	2		T
GND	GNDIO2	2			GND	GNDIO2	2		
D25	NC	-			D25	PR8B	2		C*
C25	NC	-			C25	PR8A	2		T*
D24	NC	-			D24	PR7B	2		C
B25	NC	-			B25	PR7A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H21	NC	-			H21	PR6B	2		C*
G22	NC	-			G22	PR6A	2	RDQS6	T*

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
B24	NC	-			B24	PR5B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
C24	NC	-			C24	PR5A	2		T
D23	NC	-			D23	PR4B	2		C*
C23	NC	-			C23	PR4A	2		T*
G21	PR3B	2		C	G21	PR3B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H20	PR3A	2		T	H20	PR3A	2		T
GND	GNDIO2	2			GND	GNDIO2	2		
E22	PR2B	2	VREF2_2	C*	E22	PR2B	2	VREF2_2	C*
F21	PR2A	2	VREF1_2	T*	F21	PR2A	2	VREF1_2	T*
E23	PT64B	1	VREF2_1	C	E23	PT73B	1	VREF2_1	C
GND	GNDIO1	1			GND	GNDIO1	1		
D22	PT64A	1	VREF1_1	T	D22	PT73A	1	VREF1_1	T
G20	PT63B	1		C	G20	PT72B	1		C
J18	PT63A	1		T	J18	PT72A	1		T
F20	PT62B	1		C	F20	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H19	PT62A	1		T	H19	PT71A	1		T
A24	PT61B	1		C	A24	PT70B	1		C
A23	PT61A	1		T	A23	PT70A	1		T
E21	PT60B	1		C	E21	PT69B	1		C
F19	PT60A	1		T	F19	PT69A	1		T
C22	PT59B	1		C	C22	PT68B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
E20	PT59A	1		T	E20	PT68A	1		T
B22	PT58B	1		C	B22	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
B23	PT58A	1		T	B23	PT67A	1		T
C20	PT57B	1		C	C20	PT66B	1		C
D20	PT57A	1		T	D20	PT66A	1		T
A22	PT56B	1		C	A22	PT65B	1		C
A21	PT56A	1		T	A21	PT65A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
E19	NC	-			E19	NC	-		
C19	NC	-			C19	NC	-		
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
B21	NC	-			B21	NC	-		
B20	NC	-			B20	NC	-		
D19	NC	-			D19	NC	-		
B19	NC	-			B19	NC	-		
GND	GNDIO1	1			GND	GNDIO1	1		
G17	NC	-			G17	NC	-		
E18	NC	-			E18	NC	-		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
G19	NC	-			G19	NC	-		
F17	NC	-			F17	NC	-		
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
A20	NC	-			A20	NC	-		
A19	NC	-			A19	NC	-		
E17	NC	-			E17	NC	-		
D18	NC	-			D18	NC	-		
B18	PT55B	1		C	B18	PT55B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
A18	PT55A	1		T	A18	PT55A	1		T
E16	PT54B	1		C	E16	PT54B	1		C
G16	PT54A	1		T	G16	PT54A	1		T
F16	PT53B	1		C	F16	PT53B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H18	PT53A	1		T	H18	PT53A	1		T
A17	PT52B	1		C	A17	PT52B	1		C
B17	PT52A	1		T	B17	PT52A	1		T
C18	PT51B	1		C	C18	PT51B	1		C
B16	PT51A	1		T	B16	PT51A	1		T
C17	PT50B	1		C	C17	PT50B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
D17	PT50A	1		T	D17	PT50A	1		T
E15	PT49B	1		C	E15	PT49B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
G15	PT49A	1		T	G15	PT49A	1		T
A16	PT48B	1		C	A16	PT48B	1		C
B15	PT48A	1		T	B15	PT48A	1		T
D15	PT47B	1		C	D15	PT47B	1		C
F15	PT47A	1		T	F15	PT47A	1		T
A14	PT46B	1		C	A14	PT46B	1		C
B14	PT46A	1		T	B14	PT46A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
C15	PT45B	1		C	C15	PT45B	1		C
A15	PT45A	1		T	A15	PT45A	1		T
A13	PT44B	1		C	A13	PT44B	1		C
B13	PT44A	1		T	B13	PT44A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H17	PT43B	1		C	H17	PT43B	1		C
H15	PT43A	1		T	H15	PT43A	1		T
D13	PT42B	1		C	D13	PT42B	1		C
C14	PT42A	1		T	C14	PT42A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
G14	PT41B	1		C	G14	PT41B	1		C
E14	PT41A	1		T	E14	PT41A	1		T

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A12	PT40B	1		C	A12	PT40B	1		C
B12	PT40A	1		T	B12	PT40A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
F14	PT39B	1	PCLKC1_0	C	F14	PT39B	1	PCLKC1_0	C
D14	PT39A	1	PCLKT1_0	T	D14	PT39A	1	PCLKT1_0	T
H16	XRES	1			H16	XRES	1		
H14	PT37B	0	PCLKC0_0	C	H14	PT37B	0	PCLKC0_0	C
GND	GNDIO0	0			GND	GNDIO0	0		
H13	PT37A	0	PCLKT0_0	T	H13	PT37A	0	PCLKT0_0	T
A11	PT36B	0		C	A11	PT36B	0		C
B11	PT36A	0		T	B11	PT36A	0		T
C13	PT35B	0		C	C13	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
E13	PT35A	0		T	E13	PT35A	0		T
D12	PT34B	0		C	D12	PT34B	0		C
F13	PT34A	0		T	F13	PT34A	0		T
A10	PT33B	0		C	A10	PT33B	0		C
B10	PT33A	0		T	B10	PT33A	0		T
C12	PT32B	0		C	C12	PT32B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
C10	PT32A	0		T	C10	PT32A	0		T
G13	PT31B	0		C	G13	PT31B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
H12	PT31A	0		T	H12	PT31A	0		T
A9	PT30B	0		C	A9	PT30B	0		C
B9	PT30A	0		T	B9	PT30A	0		T
E12	PT29B	0		C	E12	PT29B	0		C
G12	PT29A	0		T	G12	PT29A	0		T
A8	PT28B	0		C	A8	PT28B	0		C
B8	PT28A	0		T	B8	PT28A	0		T
GND	GNDIO0	0			GND	GNDIO0	0		
E11	PT27B	0		C	E11	PT27B	0		C
C9	PT27A	0		T	C9	PT27A	0		T
A7	PT26B	0		C	A7	PT26B	0		C
B7	PT26A	0		T	B7	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
F12	PT25B	0		C	F12	PT25B	0		C
D10	PT25A	0		T	D10	PT25A	0		T
H11	PT24B	0		C	H11	PT24B	0		C
G11	PT24A	0		T	G11	PT24A	0		T
GND	GNDIO0	0			GND	GNDIO0	0		
A6	PT23B	0		C	A6	PT23B	0		C
B6	PT23A	0		T	B6	PT23A	0		T
D8	PT22B	0		C	D8	PT22B	0		C

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
C8	PT22A	0		T	C8	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
F11	PT21B	0		C	F11	PT21B	0		C
E10	PT21A	0		T	E10	PT21A	0		T
E9	PT20B	0		C	E9	PT20B	0		C
D9	PT20A	0		T	D9	PT20A	0		T
G10	PT19B	0		C	G10	PT19B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
H10	PT19A	0		T	H10	PT19A	0		T
A5	PT18B	0		C	A5	PT18B	0		C
B5	PT18A	0		T	B5	PT18A	0		T
C7	PT17B	0		C	C7	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
D7	PT17A	0		T	D7	PT17A	0		T
E8	PT16B	0		C	E8	PT16B	0		C
F10	PT16A	0		T	F10	PT16A	0		T
F8	PT15B	0		C	F8	PT15B	0		C
H9	PT15A	0		T	H9	PT15A	0		T
C5	PT14B	0		C	C5	PT14B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
D5	PT14A	0		T	D5	PT14A	0		T
B4	PT13B	0			B4	PT13B	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
C4	PT10B	0		C	C4	PT10B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
C3	PT10A	0		T	C3	PT10A	0		T
A4	PT9B	0		C	A4	PT9B	0		C
A3	PT9A	0		T	A3	PT9A	0		T
B3	PT8B	0		C	B3	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
B2	PT8A	0		T	B2	PT8A	0		T
D4	PT7B	0		C	D4	PT7B	0		C
D3	PT7A	0		T	D3	PT7A	0		T
C2	PT6B	0		C	C2	PT6B	0		C
C1	PT6A	0		T	C1	PT6A	0		T
G8	PT5B	0		C	G8	PT5B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
G7	PT5A	0		T	G7	PT5A	0		T
E7	PT4B	0		C	E7	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
F7	PT4A	0		T	F7	PT4A	0		T
E6	PT3B	0		C	E6	PT3B	0		C
E5	PT3A	0		T	E5	PT3A	0		T
G6	PT2B	0	VREF2_0	C	G6	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	G5	PT2A	0	VREF1_0	T
L12	VCC	-			L12	VCC	-		
L13	VCC	-			L13	VCC	-		
L14	VCC	-			L14	VCC	-		
L15	VCC	-			L15	VCC	-		
M11	VCC	-			M11	VCC	-		
M12	VCC	-			M12	VCC	-		
M15	VCC	-			M15	VCC	-		
M16	VCC	-			M16	VCC	-		
N11	VCC	-			N11	VCC	-		
N16	VCC	-			N16	VCC	-		
P11	VCC	-			P11	VCC	-		
P16	VCC	-			P16	VCC	-		
R11	VCC	-			R11	VCC	-		
R12	VCC	-			R12	VCC	-		
R15	VCC	-			R15	VCC	-		
R16	VCC	-			R16	VCC	-		
T12	VCC	-			T12	VCC	-		
T13	VCC	-			T13	VCC	-		
T14	VCC	-			T14	VCC	-		
T15	VCC	-			T15	VCC	-		
D11	VCCIO0	0			D11	VCCIO0	0		
D6	VCCIO0	0			D6	VCCIO0	0		
G9	VCCIO0	0			G9	VCCIO0	0		
K12	VCCIO0	0			K12	VCCIO0	0		
J12	VCCIO0	0			J12	VCCIO0	0		
D16	VCCIO1	1			D16	VCCIO1	1		
D21	VCCIO1	1			D21	VCCIO1	1		
G18	VCCIO1	1			G18	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
K15	VCCIO1	1			K15	VCCIO1	1		
F23	VCCIO2	2			F23	VCCIO2	2		
J20	VCCIO2	2			J20	VCCIO2	2		
L23	VCCIO2	2			L23	VCCIO2	2		
M17	VCCIO2	2			M17	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
AA23	VCCIO3	3			AA23	VCCIO3	3		
R17	VCCIO3	3			R17	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
T23	VCCIO3	3			T23	VCCIO3	3		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
V20	VCCIO3	3			V20	VCCIO3	3		
AC16	VCCIO4	4			AC16	VCCIO4	4		
AC21	VCCIO4	4			AC21	VCCIO4	4		
U15	VCCIO4	4			U15	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
Y18	VCCIO4	4			Y18	VCCIO4	4		
AC11	VCCIO5	5			AC11	VCCIO5	5		
AC6	VCCIO5	5			AC6	VCCIO5	5		
U12	VCCIO5	5			U12	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
Y9	VCCIO5	5			Y9	VCCIO5	5		
AA4	VCCIO6	6			AA4	VCCIO6	6		
R10	VCCIO6	6			R10	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T4	VCCIO6	6			T4	VCCIO6	6		
V7	VCCIO6	6			V7	VCCIO6	6		
F4	VCCIO7	7			F4	VCCIO7	7		
J7	VCCIO7	7			J7	VCCIO7	7		
L4	VCCIO7	7			L4	VCCIO7	7		
M10	VCCIO7	7			M10	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
AE25	VCCIO8	8			AE25	VCCIO8	8		
V18	VCCIO8	8			V18	VCCIO8	8		
J10	VCCAUX	-			J10	VCCAUX	-		
J11	VCCAUX	-			J11	VCCAUX	-		
J16	VCCAUX	-			J16	VCCAUX	-		
J17	VCCAUX	-			J17	VCCAUX	-		
K18	VCCAUX	-			K18	VCCAUX	-		
K9	VCCAUX	-			K9	VCCAUX	-		
L18	VCCAUX	-			L18	VCCAUX	-		
L9	VCCAUX	-			L9	VCCAUX	-		
T18	VCCAUX	-			T18	VCCAUX	-		
T9	VCCAUX	-			T9	VCCAUX	-		
U18	VCCAUX	-			U18	VCCAUX	-		
U9	VCCAUX	-			U9	VCCAUX	-		
V10	VCCAUX	-			V10	VCCAUX	-		
V11	VCCAUX	-			V11	VCCAUX	-		
V16	VCCAUX	-			V16	VCCAUX	-		
V17	VCCAUX	-			V17	VCCAUX	-		
A2	GND	-			A2	GND	-		
A25	GND	-			A25	GND	-		
AA18	GND	-			AA18	GND	-		
AA24	GND	-			AA24	GND	-		
AA3	GND	-			AA3	GND	-		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AA9	GND	-			AA9	GND	-		
AD11	GND	-			AD11	GND	-		
AD16	GND	-			AD16	GND	-		
AD21	GND	-			AD21	GND	-		
AD6	GND	-			AD6	GND	-		
AE1	GND	-			AE1	GND	-		
AE26	GND	-			AE26	GND	-		
AF2	GND	-			AF2	GND	-		
AF25	GND	-			AF25	GND	-		
B1	GND	-			B1	GND	-		
B26	GND	-			B26	GND	-		
C11	GND	-			C11	GND	-		
C16	GND	-			C16	GND	-		
C21	GND	-			C21	GND	-		
C6	GND	-			C6	GND	-		
F18	GND	-			F18	GND	-		
F24	GND	-			F24	GND	-		
F3	GND	-			F3	GND	-		
F9	GND	-			F9	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J21	GND	-			J21	GND	-		
J6	GND	-			J6	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K16	GND	-			K16	GND	-		
K17	GND	-			K17	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		
L24	GND	-			L24	GND	-		
L3	GND	-			L3	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
N10	GND	-			N10	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		

LFE2-20E/20SE and LFE2-35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P17	GND	-			P17	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
T24	GND	-			T24	GND	-		
T3	GND	-			T3	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		
U13	GND	-			U13	GND	-		
U14	GND	-			U14	GND	-		
U16	GND	-			U16	GND	-		
U17	GND	-			U17	GND	-		
V13	GND	-			V13	GND	-		
V14	GND	-			V14	GND	-		
V21	GND	-			V21	GND	-		
V6	GND	-			V6	GND	-		
M3	NC	-			M3	NC	-		
N6	NC	-			N6	NC	-		
P24	NC	-			P24	NC	-		

*Supports true LVDS outputs.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D2	PL2A	7	VREF2_7	T (LVDS)*	D2	PL2A	7	VREF2_7	T (LVDS)*
D1	PL2B	7	VREF1_7	C (LVDS)*	D1	PL2B	7	VREF1_7	C (LVDS)*
GND	GNDIO7	7			GND	GNDIO7	7		
F6	PL5A	7		T	F6	PL18A	7		T
F5	PL5B	7		C	F5	PL18B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
E4	PL6A	7		T (LVDS)*	E4	PL19A	7		T (LVDS)*
E3	PL6B	7		C (LVDS)*	E3	PL19B	7		C (LVDS)*
E2	PL7A	7		T	E2	PL20A	7		T
E1	PL7B	7		C	E1	PL20B	7		C
GND	GNDIO7	7			GND	GNDIO7	7		
H6	PL8A	7	LDQS8	T (LVDS)*	H6	PL21A	7	LDQS21	T (LVDS)*
H5	PL8B	7		C (LVDS)*	H5	PL21B	7		C (LVDS)*
F2	PL9A	7		T	F2	PL22A	7		T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
F1	PL9B	7		C	F1	PL22B	7		C
H8	PL10A	7		T (LVDS)*	H8	PL23A	7		T (LVDS)*
J9	PL10B	7		C (LVDS)*	J9	PL23B	7		C (LVDS)*
G4	PL11A	7		T	G4	PL24A	7		T
GND	GNDIO7	7			GND	GNDIO7	7		
G3	PL11B	7		C	G3	PL24B	7		C
H7	PL12A	7		T (LVDS)*	H7	PL25A	7		T (LVDS)*
J8	PL12B	7		C (LVDS)*	J8	PL25B	7		C (LVDS)*
G2	PL13A	7		T	G2	PL26A	7		T
G1	PL13B	7		C	G1	PL26B	7		C
H3	PL14A	7		T (LVDS)*	H3	PL27A	7		T (LVDS)*
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
H4	PL14B	7		C (LVDS)*	H4	PL27B	7		C (LVDS)*
J5	PL15A	7		T	J5	PL28A	7		T
J4	PL15B	7		C	J4	PL28B	7		C
J3	PL16A	7	LDQS16	T (LVDS)*	J3	PL29A	7	LDQS29	T (LVDS)*
GND	GNDIO7	7			GND	GNDIO7	7		
K4	PL16B	7		C (LVDS)*	K4	PL29B	7		C (LVDS)*
H1	PL17A	7		T	H1	PL30A	7		T
H2	PL17B	7		C	H2	PL30B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
K6	PL18A	7		T (LVDS)*	K6	PL31A	7		T (LVDS)*
K7	PL18B	7		C (LVDS)*	K7	PL31B	7		C (LVDS)*
J1	PL19A	7		T	J1	PL32A	7		T
J2	PL19B	7		C	J2	PL32B	7		C
GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
K3	PL23A	7		T	K3	PL36A	7		T
K2	PL23B	7		C	K2	PL36B	7		C

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO7	7			GND	GNDIO7	7		
K1	PL24A	7		T (LVDS)*	K1	PL37A	7		T (LVDS)*
L2	PL24B	7		C (LVDS)*	L2	PL37B	7		C (LVDS)*
L1	PL25A	7	LUM0_SPLLT_IN_A	T	L1	PL38A	7	LUM0_SPLLT_IN_A	T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
M2	PL25B	7	LUM0_SPLLC_IN_A	C	M2	PL38B	7	LUM0_SPLLC_IN_A	C
M1	PL26A	7	LUM0_SPLLT_FB_A	T	M1	PL39A	7	LUM0_SPLLT_FB_A	T
N2	PL26B	7	LUM0_SPLLC_FB_A	C	N2	PL39B	7	LUM0_SPLLC_FB_A	C
GND	GNDIO7	7			GND	GNDIO7	7		
M8	VCCPLL	7			M8	NC	-		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
GND	GNDIO7	7			GND	GNDIO7	7		
N1	PL37A	7			N1	PL50A	7		
L8	PL38A	7		T	L8	PL51A	7		T
K8	PL38B	7		C	K8	PL51B	7		C
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
L6	PL39A	7		T (LVDS)*	L6	PL52A	7		T (LVDS)*
K5	PL39B	7		C (LVDS)*	K5	PL52B	7		C (LVDS)*
L7	PL40A	7		T	L7	PL53A	7		T
L5	PL40B	7		C	L5	PL53B	7		C
GND	GNDIO7	7			GND	GNDIO7	7		
P1	PL41A	7	LDQS41	T (LVDS)*	P1	PL54A	7	LDQS54	T (LVDS)*
P2	PL41B	7		C (LVDS)*	P2	PL54B	7		C (LVDS)*
M6	PL42A	7		T	M6	PL55A	7		T
VCCIO	VCCIO7	7			VCCIO	VCCIO7	7		
N8	PL42B	7		C	N8	PL55B	7		C
R1	PL43A	7		T (LVDS)*	R1	PL56A	7		T (LVDS)*
R2	PL43B	7		C (LVDS)*	R2	PL56B	7		C (LVDS)*
M7	PL44A	7	PCLKT7_0	T	M7	PL57A	7	PCLKT7_0	T
GND	GNDIO7	7			GND	GNDIO7	7		
N9	PL44B	7	PCLKC7_0	C	N9	PL57B	7	PCLKC7_0	C
M4	PL46A	6	PCLKT6_0	T (LVDS)*	M4	PL59A	6	PCLKT6_0	T (LVDS)*
M5	PL46B	6	PCLKC6_0	C (LVDS)*	M5	PL59B	6	PCLKC6_0	C (LVDS)*
N7	PL47A	6	VREF2_6	T	N7	PL60A	6	VREF2_6	T
P9	PL47B	6	VREF1_6	C	P9	PL60B	6	VREF1_6	C
N3	PL48A	6		T (LVDS)*	N3	PL61A	6		T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
N4	PL48B	6		C (LVDS)*	N4	PL61B	6		C (LVDS)*
N5	PL49A	6		T	N5	PL62A	6		T
P7	PL49B	6		C	P7	PL62B	6		C
T1	PL50A	6	LDQS50	T (LVDS)*	T1	PL63A	6	LDQS63	T (LVDS)*
GND	GNDIO6	6			GND	GNDIO6	6		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
T2	PL50B	6		C (LVDS)*	T2	PL63B	6		C (LVDS)*
P8	PL51A	6		T	P8	PL64A	6		T
P6	PL51B	6		C	P6	PL64B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
P5	PL52A	6		T (LVDS)*	P5	PL65A	6		T (LVDS)*
P4	PL52B	6		C (LVDS)*	P4	PL65B	6		C (LVDS)*
U1	PL53A	6		T	U1	PL66A	6		T
V1	PL53B	6		C	V1	PL66B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
P3	PL54A	6		T (LVDS)*	P3	PL67A	6		T (LVDS)*
R3	PL54B	6		C (LVDS)*	R3	PL67B	6		C (LVDS)*
R4	PL55A	6		T	R4	PL68A	6		T
U2	PL55B	6		C	U2	PL68B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
V2	PL56A	6		T (LVDS)*	V2	PL69A	6		T (LVDS)*
W2	PL56B	6		C (LVDS)*	W2	PL69B	6		C (LVDS)*
T6	PL57A	6		T	T6	PL70A	6		T
R5	PL57B	6		C	R5	PL70B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
R6	PL58A	6	LDQS58	T (LVDS)*	R6	PL71A	6	LDQS71	T (LVDS)*
R7	PL58B	6		C (LVDS)*	R7	PL71B	6		C (LVDS)*
W1	PL59A	6		T	W1	PL72A	6		T
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
Y2	PL59B	6		C	Y2	PL72B	6		C
Y1	PL60A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	Y1	PL73A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
AA2	PL60B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	AA2	PL73B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
T5	PL61A	6	LLM0_GDLLT_FB_A	T	T5	PL74A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO6	6			GND	GNDIO6	6		
T7	PL61B	6	LLM0_GDLLC_FB_D	C	T7	PL74B	6	LLM0_GDLLC_FB_D	C
R8	VCCPLL	6			R8	VCCPLL	-		
T8	LLM0_PLLCAP	6			T8	LLM0_PLLCAP	6		
U3	PL63A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	U3	PL76A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
U4	PL63B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	U4	PL76B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
V3	PL64A	6	LLM0_GPLLT_FB_A	T	V3	PL77A	6	LLM0_GPLLT_FB_A	T
U5	PL64B	6	LLM0_GPLLC_FB_A	C	U5	PL77B	6	LLM0_GPLLC_FB_A	C
V4	PL65A	6		T (LVDS)*	V4	PL78A	6		T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
V5	PL65B	6		C (LVDS)*	V5	PL78B	6		C (LVDS)*
Y3	PL66A	6		T	Y3	PL79A	6		T
Y4	PL66B	6		C	Y4	PL79B	6		C
W3	PL67A	6	LDQS67	T (LVDS)*	W3	PL80A	6	LDQS80	T (LVDS)*
GND	GNDIO6	6			GND	GNDIO6	6		
W4	PL67B	6		C (LVDS)*	W4	PL80B	6		C (LVDS)*
AA1	PL68A	6		T	AA1	PL81A	6		T

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AB1	PL68B	6		C	AB1	PL81B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
U8	PL69A	6		T (LVDS)*	U8	PL82A	6		T (LVDS)*
U7	PL69B	6		C (LVDS)*	U7	PL82B	6		C (LVDS)*
V8	PL70A	6		T	V8	PL83A	6		T
U6	PL70B	6		C	U6	PL83B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
W6	PL71A	6		T (LVDS)*	W6	PL84A	6		T (LVDS)*
W5	PL71B	6		C (LVDS)*	W5	PL84B	6		C (LVDS)*
AC1	PL72A	6		T	AC1	PL85A	6		T
AD1	PL72B	6		C	AD1	PL85B	6		C
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
Y6	PL73A	6		T (LVDS)*	Y6	PL86A	6		T (LVDS)*
Y5	PL73B	6		C (LVDS)*	Y5	PL86B	6		C (LVDS)*
AE2	PL74A	6		T	AE2	PL87A	6		T
AD2	PL74B	6		C	AD2	PL87B	6		C
GND	GNDIO6	6			GND	GNDIO6	6		
AB3	PL75A	6	LDQS75	T (LVDS)*	AB3	PL88A	6	LDQS88	T (LVDS)*
AB2	PL75B	6		C (LVDS)*	AB2	PL88B	6		C (LVDS)*
W7	PL76A	6		T	W7	PL89A	6		T
VCCIO	VCCIO6	6			VCCIO	VCCIO6	6		
W8	PL76B	6		C	W8	PL89B	6		C
Y7	PL77A	6		T (LVDS)*	Y7	PL90A	6		T (LVDS)*
Y8	PL77B	6		C (LVDS)*	Y8	PL90B	6		C (LVDS)*
AC2	PL78A	6		T	AC2	PL91A	6		T
GND	GNDIO6	6			GND	GNDIO6	6		
AD3	PL78B	6		C	AD3	PL91B	6		C
AC3	TCK	-			AC3	TCK	-		
AA8	TDI	-			AA8	TDI	-		
AB4	TMS	-			AB4	TMS	-		
AA5	TDO	-			AA5	TDO	-		
AB5	VCCJ	-			AB5	VCCJ	-		
AE3	PB2A	5	VREF2_5	T	AE3	PB2A	5	VREF2_5	T
AF3	PB2B	5	VREF1_5	C	AF3	PB2B	5	VREF1_5	C
AC4	PB3A	5		T	AC4	PB3A	5		T
AD4	PB3B	5		C	AD4	PB3B	5		C
AE4	PB4A	5		T	AE4	PB4A	5		T
AF4	PB4B	5		C	AF4	PB4B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
V9	PB5A	5		T	V9	PB5A	5		T
W9	PB5B	5		C	W9	PB5B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AA6	PB6A	5	BDQS6	T	AA6	PB6A	5	BDQS6	T
AB6	PB6B	5		C	AB6	PB6B	5		C

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AC5	PB7A	5		T	AC5	PB7A	5		T
AD5	PB7B	5		C	AD5	PB7B	5		C
AA7	PB8A	5		T	AA7	PB8A	5		T
AB7	PB8B	5		C	AB7	PB8B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AE5	PB9A	5		T	AE5	PB9A	5		T
AF5	PB9B	5		C	AF5	PB9B	5		C
AC7	PB10A	5		T	AC7	PB10A	5		T
AD7	PB10B	5		C	AD7	PB10B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
W10	PB20A	5		T	W10	PB29A	5		T
Y10	PB20B	5		C	Y10	PB29B	5		C
W11	PB21A	5		T	W11	PB30A	5		T
AA10	PB21B	5		C	AA10	PB30B	5		C
AC8	PB22A	5		T	AC8	PB31A	5		T
AD8	PB22B	5		C	AD8	PB31B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AB8	PB23A	5		T	AB8	PB32A	5		T
AB10	PB23B	5		C	AB10	PB32B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AE6	PB24A	5	BDQS24	T	AE6	PB33A	5	BDQS33	T
AF6	PB24B	5		C	AF6	PB33B	5		C
AA11	PB25A	5		T	AA11	PB34A	5		T
AC9	PB25B	5		C	AC9	PB34B	5		C
AB9	PB26A	5		T	AB9	PB35A	5		T
AD9	PB26B	5		C	AD9	PB35B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y11	PB27A	5		T	Y11	PB36A	5		T
AB11	PB27B	5		C	AB11	PB36B	5		C
AE7	PB28A	5		T	AE7	PB37A	5		T
AF7	PB28B	5		C	AF7	PB37B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AC10	PB29A	5		T	AC10	PB38A	5		T
AD10	PB29B	5		C	AD10	PB38B	5		C
AA12	PB30A	5		T	AA12	PB39A	5		T
W12	PB30B	5		C	W12	PB39B	5		C
AB12	PB31A	5		T	AB12	PB40A	5		T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y12	PB31B	5		C	Y12	PB40B	5		C
AD12	PB32A	5		T	AD12	PB41A	5		T

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AC12	PB32B	5		C	AC12	PB41B	5		C
AC13	PB33A	5	BDQS33	T	AC13	PB42A	5	BDQS42	T
GND	GNDIO5	5			GND	GNDIO5	5		
AA13	PB33B	5		C	AA13	PB42B	5		C
AD13	PB34A	5		T	AD13	PB43A	5		T
AC14	PB34B	5		C	AC14	PB43B	5		C
AE8	PB35A	5		T	AE8	PB44A	5		T
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
AF8	PB35B	5		C	AF8	PB44B	5		C
AB15	PB36A	5		T	AB15	PB45A	5		T
Y13	PB36B	5		C	Y13	PB45B	5		C
AE9	PB37A	5		T	AE9	PB46A	5		T
GND	GNDIO5	5			GND	GNDIO5	5		
AF9	PB37B	5		C	AF9	PB46B	5		C
W13	PB38A	5		T	W13	PB47A	5		T
AA14	PB38B	5		C	AA14	PB47B	5		C
AE10	PB39A	5		T	AE10	PB48A	5		T
AF10	PB39B	5		C	AF10	PB48B	5		C
W14	PB40A	5		T	W14	PB49A	5		T
AB13	PB40B	5		C	AB13	PB49B	5		C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
Y14	PB41A	5		T	Y14	PB50A	5		T
AB14	PB41B	5		C	AB14	PB50B	5		C
GND	GNDIO5	5			GND	GNDIO5	5		
AE11	PB42A	5	BDQS42	T	AE11	PB51A	5	BDQS51	T
AF11	PB42B	5		C	AF11	PB51B	5		C
AD14	PB43A	5		T	AD14	PB52A	5		T
AA15	PB43B	5		C	AA15	PB52B	5		C
AE12	PB44A	5	PCLKT5_0	T	AE12	PB53A	5	PCLKT5_0	T
AF12	PB44B	5	PCLKC5_0	C	AF12	PB53B	5	PCLKC5_0	C
VCCIO	VCCIO5	5			VCCIO	VCCIO5	5		
GND	GNDIO5	5			GND	GNDIO5	5		
AD15	PB49A	4	PCLKT4_0	T	AD15	PB58A	4	PCLKT4_0	T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AC15	PB49B	4	PCLKC4_0	C	AC15	PB58B	4	PCLKC4_0	C
AE13	PB50A	4		T	AE13	PB59A	4		T
AF13	PB50B	4		C	AF13	PB59B	4		C
AB17	PB51A	4	BDQS51	T	AB17	PB60A	4	BDQS60	T
GND	GNDIO4	4			GND	GNDIO4	4		
Y15	PB51B	4		C	Y15	PB60B	4		C
AE14	PB52A	4		T	AE14	PB61A	4		T
AF14	PB52B	4		C	AF14	PB61B	4		C
AA16	PB53A	4		T	AA16	PB62A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
W15	PB53B	4		C	W15	PB62B	4		C
AC17	PB54A	4		T	AC17	PB63A	4		T
AB16	PB54B	4		C	AB16	PB63B	4		C
AE15	PB55A	4		T	AE15	PB64A	4		T
GND	GNDIO4	4			GND	GNDIO4	4		
AF15	PB55B	4		C	AF15	PB64B	4		C
AE16	PB56A	4		T	AE16	PB65A	4		T
AF16	PB56B	4		C	AF16	PB65B	4		C
Y16	PB57A	4		T	Y16	PB66A	4		T
AB18	PB57B	4		C	AB18	PB66B	4		C
AD17	PB58A	4		T	AD17	PB67A	4		T
AD18	PB58B	4		C	AD18	PB67B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AC18	PB59A	4		T	AC18	PB68A	4		T
AD19	PB59B	4		C	AD19	PB68B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AC19	PB60A	4	BDQS60	T	AC19	PB69A	4	BDQS69	T
AE17	PB60B	4		C	AE17	PB69B	4		C
AB19	PB61A	4		T	AB19	PB70A	4		T
AE19	PB61B	4		C	AE19	PB70B	4		C
AF17	PB62A	4		T	AF17	PB71A	4		T
AE18	PB62B	4		C	AE18	PB71B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
W16	PB63A	4		T	W16	PB72A	4		T
AA17	PB63B	4		C	AA17	PB72B	4		C
AF18	PB64A	4		T	AF18	PB73A	4		T
AF19	PB64B	4		C	AF19	PB73B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AA19	PB65A	4		T	AA19	PB74A	4		T
W17	PB65B	4		C	W17	PB74B	4		C
Y19	PB66A	4		T	Y19	PB75A	4		T
Y17	PB66B	4		C	Y17	PB75B	4		C
AF20	PB67A	4		T	AF20	PB76A	4		T
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AE20	PB67B	4		C	AE20	PB76B	4		C
AA20	PB68A	4		T	AA20	PB77A	4		T
W18	PB68B	4		C	W18	PB77B	4		C
AD20	PB69A	4	BDQS69	T	AD20	PB78A	4	BDQS78	T
GND	GNDIO4	4			GND	GNDIO4	4		
AE21	PB69B	4		C	AE21	PB78B	4		C
AF21	PB70A	4		T	AF21	PB79A	4		T
AF22	PB70B	4		C	AF22	PB79B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
GND	GNDIO4	4			GND	GNDIO4	4		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AE22	PB74A	4		T	AE22	PB92A	4		T
AD22	PB74B	4		C	AD22	PB92B	4		C
AF23	PB75A	4		T	AF23	PB93A	4		T
AE23	PB75B	4		C	AE23	PB93B	4		C
AD23	PB76A	4		T	AD23	PB94A	4		T
AC23	PB76B	4		C	AC23	PB94B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
AB20	PB77A	4		T	AB20	PB95A	4		T
AC20	PB77B	4		C	AC20	PB95B	4		C
GND	GNDIO4	4			GND	GNDIO4	4		
AB21	PB78A	4	BDQS78	T	AB21	PB96A	4	BDQS96	T
AC22	PB78B	4		C	AC22	PB96B	4		C
W19	PB79A	4		T	W19	PB97A	4		T
AA21	PB79B	4		C	AA21	PB97B	4		C
AF24	PB80A	4		T	AF24	PB98A	4		T
AE24	PB80B	4		C	AE24	PB98B	4		C
VCCIO	VCCIO4	4			VCCIO	VCCIO4	4		
Y20	PB81A	4		T	Y20	PB99A	4		T
AB22	PB81B	4		C	AB22	PB99B	4		C
Y21	PB82A	4	VREF2_4	T	Y21	PB100A	4	VREF2_4	T
AB23	PB82B	4	VREF1_4	C	AB23	PB100B	4	VREF1_4	C
GND	GNDIO4	4			GND	GNDIO4	4		
AD24	CFG2	8			AD24	CFG2	8		
W20	CFG1	8			W20	CFG1	8		
AC24	CFG0	8			AC24	CFG0	8		
V19	PROGRAMN	8			V19	PROGRAMN	8		
AA22	CCLK	8			AA22	CCLK	8		
AB24	INITN	8			AB24	INITN	8		
AD25	DONE	8			AD25	DONE	8		
GND	GNDIO8	8			GND	GNDIO8	8		
W21	PR77B	8	WRITEN	C	W21	PR90B	8	WRITEN	C
Y22	PR77A	8	CS1N	T	Y22	PR90A	8	CS1N	T
AC25	PR76B	8	CSN	C	AC25	PR89B	8	CSN	C
AB25	PR76A	8	D0	T	AB25	PR89A	8	D0	T
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		
AD26	PR75B	8	D1	C	AD26	PR88B	8	D1	C
AC26	PR75A	8	D2	T	AC26	PR88A	8	D2	T
Y23	PR74B	8	D3	C	Y23	PR87B	8	D3	C
GND	GNDIO8	8			GND	GNDIO8	8		
W22	PR74A	8	D4	T	W22	PR87A	8	D4	T
AA25	PR73B	8	D5	C	AA25	PR86B	8	D5	C
AB26	PR73A	8	D6	T	AB26	PR86A	8	D6	T
W23	PR72B	8	D7	C	W23	PR85B	8	D7	C
VCCIO	VCCIO8	8			VCCIO	VCCIO8	8		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
V22	PR72A	8	DI/CSSPI0N	T	V22	PR85A	8	DI/CSSPI0N	T
Y24	PR71B	8	DOUT/CSON	C	Y24	PR84B	8	DOUT/CSON	C
Y25	PR71A	8	BUSY/SISPI	T	Y25	PR84A	8	BUSY/SISPI	T
W24	PR70B	3		C	W24	PR83B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
V23	PR70A	3		T	V23	PR83A	3		T
AA26	PR69B	3		C (LVDS)*	AA26	PR82B	3		C (LVDS)*
Y26	PR69A	3		T (LVDS)*	Y26	PR82A	3		T (LVDS)*
U21	PR68B	3		C	U21	PR81B	3		C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
U19	PR68A	3		T	U19	PR81A	3		T
W25	PR67B	3		C (LVDS)*	W25	PR80B	3		C (LVDS)*
W26	PR67A	3	RDQS67	T (LVDS)*	W26	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	3			GND	GNDIO3	3		
V24	PR66B	3		C	V24	PR79B	3		C
V25	PR66A	3		T	V25	PR79A	3		T
V26	PR65B	3		C (LVDS)*	V26	PR78B	3		C (LVDS)*
U26	PR65A	3		T (LVDS)*	U26	PR78A	3		T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
U22	PR64B	3	RLM0_GPLLC_FB_A	C	U22	PR77B	3	RLM0_GPLLC_FB_A	C
U23	PR64A	3	RLM0_GPLLT_FB_A	T	U23	PR77A	3	RLM0_GPLLT_FB_A	T
U24	PR63B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	U24	PR76B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
U25	PR63A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	U25	PR76A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
R20	RLM0_PLLCAP	3			R20	RLM0_PLLCAP	3		
P18	VCCPLL	3			P18	VCCPLL	-		
T19	PR61B	3	RLM0_GDLLC_FB_A	C	T19	PR74B	3	RLM0_GDLLC_FB_A	C
U20	PR61A	3	RLM0_GDLLT_FB_A	T	U20	PR74A	3	RLM0_GDLLT_FB_A	T
GND	GNDIO3	3			GND	GNDIO3	3		
T25	PR60B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	T25	PR73B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
T26	PR60A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	T26	PR73A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
T20	PR59B	3		C	T20	PR72B	3		C
T22	PR59A	3		T	T22	PR72A	3		T
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R26	PR58B	3		C (LVDS)*	R26	PR71B	3		C (LVDS)*
R25	PR58A	3	RDQS58	T (LVDS)*	R25	PR71A	3	RDQS71	T (LVDS)*
R22	PR57B	3		C	R22	PR70B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
T21	PR57A	3		T	T21	PR70A	3		T
P26	PR56B	3		C (LVDS)*	P26	PR69B	3		C (LVDS)*
P25	PR56A	3		T (LVDS)*	P25	PR69A	3		T (LVDS)*
R24	PR55B	3		C	R24	PR68B	3		C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R23	PR55A	3		T	R23	PR68A	3		T
P20	PR54B	3		C (LVDS)*	P20	PR67B	3		C (LVDS)*

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
R19	PR54A	3		T (LVDS)*	R19	PR67A	3		T (LVDS)*
P21	PR53B	3		C	P21	PR66B	3		C
GND	GNDIO3	3			GND	GNDIO3	3		
P19	PR53A	3		T	P19	PR66A	3		T
P23	PR52B	3		C (LVDS)*	P23	PR65B	3		C (LVDS)*
P22	PR52A	3		T (LVDS)*	P22	PR65A	3		T (LVDS)*
N22	PR51B	3		C	N22	PR64B	3		C
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
R21	PR51A	3		T	R21	PR64A	3		T
N26	PR50B	3		C (LVDS)*	N26	PR63B	3		C (LVDS)*
N25	PR50A	3	RDQS50	T (LVDS)*	N25	PR63A	3	RDQS63	T (LVDS)*
GND	GNDIO3	3			GND	GNDIO3	3		
N19	PR49B	3		C	N19	PR62B	3		C
N20	PR49A	3		T	N20	PR62A	3		T
M26	PR48B	3		C (LVDS)*	M26	PR61B	3		C (LVDS)*
M25	PR48A	3		T (LVDS)*	M25	PR61A	3		T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	VCCIO3	3		
N18	PR47B	3	VREF2_3	C	N18	PR60B	3	VREF2_3	C
N21	PR47A	3	VREF1_3	T	N21	PR60A	3	VREF1_3	T
L26	PR46B	3	PCLKC3_0	C (LVDS)*	L26	PR59B	3	PCLKC3_0	C (LVDS)*
L25	PR46A	3	PCLKT3_0	T (LVDS)*	L25	PR59A	3	PCLKT3_0	T (LVDS)*
N24	PR44B	2	PCLKC2_0	C	N24	PR57B	2	PCLKC2_0	C
M23	PR44A	2	PCLKT2_0	T	M23	PR57A	2	PCLKT2_0	T
GND	GNDIO2	2			GND	GNDIO2	2		
L21	PR43B	2		C (LVDS)*	L21	PR56B	2		C (LVDS)*
K22	PR43A	2		T (LVDS)*	K22	PR56A	2		T (LVDS)*
M24	PR42B	2		C	M24	PR55B	2		C
N23	PR42A	2		T	N23	PR55A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
K26	PR41B	2		C (LVDS)*	K26	PR54B	2		C (LVDS)*
K25	PR41A	2	RDQS41	T (LVDS)*	K25	PR54A	2	RDQS54	T (LVDS)*
M20	PR40B	2		C	M20	PR53B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
M19	PR40A	2		T	M19	PR53A	2		T
L22	PR39B	2		C (LVDS)*	L22	PR52B	2		C (LVDS)*
M22	PR39A	2		T (LVDS)*	M22	PR52A	2		T (LVDS)*
K21	PR38B	2		C	K21	PR51B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
M21	PR38A	2		T	M21	PR51A	2		T
K24	PR37B	2		C (LVDS)*	K24	PR50B	2		C (LVDS)*
J24	PR37A	2		T (LVDS)*	J24	PR50A	2		T (LVDS)*
GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
GND	GNDIO2	2			GND	GNDIO2	2		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
L20	VCCPLL	2			L20	NC	-		
GND	GNDIO2	2			GND	GNDIO2	2		
J26	PR26B	2	RUM0_SPLLC_FB_A	C	J26	PR39B	2	RUM0_SPLLC_FB_A	C
J25	PR26A	2	RUM0_SPLLT_FB_A	T	J25	PR39A	2	RUM0_SPLLT_FB_A	T
J23	PR25B	2	RUM0_SPLLC_IN_A	C	J23	PR38B	2	RUM0_SPLLC_IN_A	C
K23	PR25A	2	RUM0_SPLLT_IN_A	T	K23	PR38A	2	RUM0_SPLLT_IN_A	T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H26	PR24B	2		C (LVDS)*	H26	PR37B	2		C (LVDS)*
H25	PR24A	2		T (LVDS)*	H25	PR37A	2		T (LVDS)*
H24	PR23B	2		C	H24	PR36B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
H23	PR23A	2		T	H23	PR36A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
G26	PR19B	2		C	G26	PR32B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
G25	PR19A	2		T	G25	PR32A	2		T
F26	PR18B	2		C (LVDS)*	F26	PR31B	2		C (LVDS)*
F25	PR18A	2		T (LVDS)*	F25	PR31A	2		T (LVDS)*
K20	PR17B	2		C	K20	PR30B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
L19	PR17A	2		T	L19	PR30A	2		T
E26	PR16B	2		C (LVDS)*	E26	PR29B	2		C (LVDS)*
E25	PR16A	2	RDQS16	T (LVDS)*	E25	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	2			GND	GNDIO2	2		
J22	PR15B	2		C	J22	PR28B	2		C
H22	PR15A	2		T	H22	PR28A	2		T
G24	PR14B	2		C (LVDS)*	G24	PR27B	2		C (LVDS)*
G23	PR14A	2		T (LVDS)*	G23	PR27A	2		T (LVDS)*
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
K19	PR13B	2		C	K19	PR26B	2		C
J19	PR13A	2		T	J19	PR26A	2		T
D26	PR12B	2		C (LVDS)*	D26	PR25B	2		C (LVDS)*
C26	PR12A	2		T (LVDS)*	C26	PR25A	2		T (LVDS)*
F22	PR11B	2		C	F22	PR24B	2		C
E24	PR11A	2		T	E24	PR24A	2		T
GND	GNDIO2	2			GND	GNDIO2	2		
D25	PR10B	2		C (LVDS)*	D25	PR23B	2		C (LVDS)*
C25	PR10A	2		T (LVDS)*	C25	PR23A	2		T (LVDS)*
D24	PR9B	2		C	D24	PR22B	2		C
B25	PR9A	2		T	B25	PR22A	2		T
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H21	PR8B	2		C (LVDS)*	H21	PR21B	2		C (LVDS)*
G22	PR8A	2	RDQS8	T (LVDS)*	G22	PR21A	2	RDQS21	T (LVDS)*

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
B24	PR7B	2		C	B24	PR20B	2		C
GND	GNDIO2	2			GND	GNDIO2	2		
C24	PR7A	2		T	C24	PR20A	2		T
D23	PR6B	2		C (LVDS)*	D23	PR19B	2		C (LVDS)*
C23	PR6A	2		T (LVDS)*	C23	PR19A	2		T (LVDS)*
G21	PR5B	2		C	G21	PR18B	2		C
VCCIO	VCCIO2	2			VCCIO	VCCIO2	2		
H20	PR5A	2		T	H20	PR18A	2		T
GND	GNDIO2	2			GND	GNDIO2	2		
E22	PR2B	2	VREF2_2	C (LVDS)*	E22	PR2B	2	VREF2_2	C (LVDS)*
F21	PR2A	2	VREF1_2	T (LVDS)*	F21	PR2A	2	VREF1_2	T (LVDS)*
E23	PT82B	1	VREF2_1	C	E23	PT100B	1	VREF2_1	C
GND	GNDIO1	1			GND	GNDIO1	1		
D22	PT82A	1	VREF1_1	T	D22	PT100A	1	VREF1_1	T
G20	PT81B	1		C	G20	PT99B	1		C
J18	PT81A	1		T	J18	PT99A	1		T
F20	PT80B	1		C	F20	PT98B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H19	PT80A	1		T	H19	PT98A	1		T
A24	PT79B	1		C	A24	PT97B	1		C
A23	PT79A	1		T	A23	PT97A	1		T
E21	PT78B	1		C	E21	PT96B	1		C
F19	PT78A	1		T	F19	PT96A	1		T
C22	PT77B	1		C	C22	PT95B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
E20	PT77A	1		T	E20	PT95A	1		T
B22	PT76B	1		C	B22	PT94B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
B23	PT76A	1		T	B23	PT94A	1		T
C20	PT75B	1		C	C20	PT93B	1		C
D20	PT75A	1		T	D20	PT93A	1		T
A22	PT74B	1		C	A22	PT92B	1		C
A21	PT74A	1		T	A21	PT92A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
E19	PT71B	1		C	E19	PT85B	1		C
C19	PT71A	1		T	C19	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
B21	PT70B	1		C	B21	PT79B	1		C
B20	PT70A	1		T	B20	PT79A	1		T
D19	PT69B	1		C	D19	PT78B	1		C
B19	PT69A	1		T	B19	PT78A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
G17	PT68B	1		C	G17	PT77B	1		C
E18	PT68A	1		T	E18	PT77A	1		T

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
G19	PT67B	1		C	G19	PT76B	1		C
F17	PT67A	1		T	F17	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
A20	PT66B	1		C	A20	PT75B	1		C
A19	PT66A	1		T	A19	PT75A	1		T
E17	PT65B	1		C	E17	PT74B	1		C
D18	PT65A	1		T	D18	PT74A	1		T
B18	PT64B	1		C	B18	PT73B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
A18	PT64A	1		T	A18	PT73A	1		T
E16	PT63B	1		C	E16	PT72B	1		C
G16	PT63A	1		T	G16	PT72A	1		T
F16	PT62B	1		C	F16	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H18	PT62A	1		T	H18	PT71A	1		T
A17	PT61B	1		C	A17	PT70B	1		C
B17	PT61A	1		T	B17	PT70A	1		T
C18	PT60B	1		C	C18	PT69B	1		C
B16	PT60A	1		T	B16	PT69A	1		T
C17	PT59B	1		C	C17	PT68B	1		C
GND	GNDIO1	1			GND	GNDIO1	1		
D17	PT59A	1		T	D17	PT68A	1		T
E15	PT58B	1		C	E15	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
G15	PT58A	1		T	G15	PT67A	1		T
A16	PT57B	1		C	A16	PT66B	1		C
B15	PT57A	1		T	B15	PT66A	1		T
D15	PT56B	1		C	D15	PT65B	1		C
F15	PT56A	1		T	F15	PT65A	1		T
A14	PT55B	1		C	A14	PT64B	1		C
B14	PT55A	1		T	B14	PT64A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
C15	PT54B	1		C	C15	PT63B	1		C
A15	PT54A	1		T	A15	PT63A	1		T
A13	PT53B	1		C	A13	PT62B	1		C
B13	PT53A	1		T	B13	PT62A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
H17	PT52B	1		C	H17	PT61B	1		C
H15	PT52A	1		T	H15	PT61A	1		T
D13	PT51B	1		C	D13	PT60B	1		C
C14	PT51A	1		T	C14	PT60A	1		T
GND	GNDIO1	1			GND	GNDIO1	1		
G14	PT50B	1		C	G14	PT59B	1		C
E14	PT50A	1		T	E14	PT59A	1		T

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A12	PT49B	1		C	A12	PT58B	1		C
B12	PT49A	1		T	B12	PT58A	1		T
VCCIO	VCCIO1	1			VCCIO	VCCIO1	1		
F14	PT48B	1	PCLKC1_0	C	F14	PT57B	1	PCLKC1_0	C
D14	PT48A	1	PCLKT1_0	T	D14	PT57A	1	PCLKT1_0	T
H16	XRES	1			H16	XRES	1		
H14	PT46B	0	PCLKC0_0	C	H14	PT55B	0	PCLKC0_0	C
GND	GNDIO0	0			GND	GNDIO0	0		
H13	PT46A	0	PCLKT0_0	T	H13	PT55A	0	PCLKT0_0	T
A11	PT45B	0		C	A11	PT54B	0		C
B11	PT45A	0		T	B11	PT54A	0		T
C13	PT44B	0		C	C13	PT53B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
E13	PT44A	0		T	E13	PT53A	0		T
D12	PT43B	0		C	D12	PT52B	0		C
F13	PT43A	0		T	F13	PT52A	0		T
A10	PT42B	0		C	A10	PT51B	0		C
B10	PT42A	0		T	B10	PT51A	0		T
C12	PT41B	0		C	C12	PT50B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
C10	PT41A	0		T	C10	PT50A	0		T
G13	PT40B	0		C	G13	PT49B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
H12	PT40A	0		T	H12	PT49A	0		T
A9	PT39B	0		C	A9	PT48B	0		C
B9	PT39A	0		T	B9	PT48A	0		T
E12	PT38B	0		C	E12	PT47B	0		C
G12	PT38A	0		T	G12	PT47A	0		T
A8	PT37B	0		C	A8	PT46B	0		C
B8	PT37A	0		T	B8	PT46A	0		T
GND	GNDIO0	0			GND	GNDIO0	0		
E11	PT36B	0		C	E11	PT45B	0		C
C9	PT36A	0		T	C9	PT45A	0		T
A7	PT35B	0		C	A7	PT44B	0		C
B7	PT35A	0		T	B7	PT44A	0		T
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
F12	PT34B	0		C	F12	PT43B	0		C
D10	PT34A	0		T	D10	PT43A	0		T
H11	PT33B	0		C	H11	PT42B	0		C
G11	PT33A	0		T	G11	PT42A	0		T
GND	GNDIO0	0			GND	GNDIO0	0		
A6	PT32B	0		C	A6	PT41B	0		C
B6	PT32A	0		T	B6	PT41A	0		T
D8	PT31B	0		C	D8	PT40B	0		C

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
C8	PT31A	0		T	C8	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
F11	PT30B	0		C	F11	PT39B	0		C
E10	PT30A	0		T	E10	PT39A	0		T
E9	PT29B	0		C	E9	PT38B	0		C
D9	PT29A	0		T	D9	PT38A	0		T
G10	PT28B	0		C	G10	PT37B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
H10	PT28A	0		T	H10	PT37A	0		T
A5	PT27B	0		C	A5	PT36B	0		C
B5	PT27A	0		T	B5	PT36A	0		T
C7	PT26B	0		C	C7	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
D7	PT26A	0		T	D7	PT35A	0		T
E8	PT25B	0		C	E8	PT34B	0		C
F10	PT25A	0		T	F10	PT34A	0		T
F8	PT24B	0		C	F8	PT33B	0		C
H9	PT24A	0		T	H9	PT33A	0		T
C5	PT23B	0		C	C5	PT32B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
D5	PT23A	0		T	D5	PT32A	0		T
B4	PT22B	0			B4	PT31B	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
C4	PT10B	0		C	C4	PT10B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
C3	PT10A	0		T	C3	PT10A	0		T
A4	PT9B	0		C	A4	PT9B	0		C
A3	PT9A	0		T	A3	PT9A	0		T
B3	PT8B	0		C	B3	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		
B2	PT8A	0		T	B2	PT8A	0		T
D4	PT7B	0		C	D4	PT7B	0		C
D3	PT7A	0		T	D3	PT7A	0		T
C2	PT6B	0		C	C2	PT6B	0		C
C1	PT6A	0		T	C1	PT6A	0		T
G8	PT5B	0		C	G8	PT5B	0		C
GND	GNDIO0	0			GND	GNDIO0	0		
G7	PT5A	0		T	G7	PT5A	0		T
E7	PT4B	0		C	E7	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	VCCIO0	0		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
F7	PT4A	0		T	F7	PT4A	0		T
E6	PT3B	0		C	E6	PT3B	0		C
E5	PT3A	0		T	E5	PT3A	0		T
G6	PT2B	0	VREF2_0	C	G6	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	G5	PT2A	0	VREF1_0	T
L12	VCC	-			L12	VCC	-		
L13	VCC	-			L13	VCC	-		
L14	VCC	-			L14	VCC	-		
L15	VCC	-			L15	VCC	-		
M11	VCC	-			M11	VCC	-		
M12	VCC	-			M12	VCC	-		
M15	VCC	-			M15	VCC	-		
M16	VCC	-			M16	VCC	-		
N11	VCC	-			N11	VCC	-		
N16	VCC	-			N16	VCC	-		
P11	VCC	-			P11	VCC	-		
P16	VCC	-			P16	VCC	-		
R11	VCC	-			R11	VCC	-		
R12	VCC	-			R12	VCC	-		
R15	VCC	-			R15	VCC	-		
R16	VCC	-			R16	VCC	-		
T12	VCC	-			T12	VCC	-		
T13	VCC	-			T13	VCC	-		
T14	VCC	-			T14	VCC	-		
T15	VCC	-			T15	VCC	-		
D11	VCCIO0	0			D11	VCCIO0	0		
D6	VCCIO0	0			D6	VCCIO0	0		
G9	VCCIO0	0			G9	VCCIO0	0		
K12	VCCIO0	0			K12	VCCIO0	0		
J12	VCCIO0	0			J12	VCCIO0	0		
D16	VCCIO1	1			D16	VCCIO1	1		
D21	VCCIO1	1			D21	VCCIO1	1		
G18	VCCIO1	1			G18	VCCIO1	1		
J15	VCCIO1	1			J15	VCCIO1	1		
K15	VCCIO1	1			K15	VCCIO1	1		
F23	VCCIO2	2			F23	VCCIO2	2		
J20	VCCIO2	2			J20	VCCIO2	2		
L23	VCCIO2	2			L23	VCCIO2	2		
M17	VCCIO2	2			M17	VCCIO2	2		
M18	VCCIO2	2			M18	VCCIO2	2		
AA23	VCCIO3	3			AA23	VCCIO3	3		
R17	VCCIO3	3			R17	VCCIO3	3		
R18	VCCIO3	3			R18	VCCIO3	3		
T23	VCCIO3	3			T23	VCCIO3	3		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
V20	VCCIO3	3			V20	VCCIO3	3		
AC16	VCCIO4	4			AC16	VCCIO4	4		
AC21	VCCIO4	4			AC21	VCCIO4	4		
U15	VCCIO4	4			U15	VCCIO4	4		
V15	VCCIO4	4			V15	VCCIO4	4		
Y18	VCCIO4	4			Y18	VCCIO4	4		
AC11	VCCIO5	5			AC11	VCCIO5	5		
AC6	VCCIO5	5			AC6	VCCIO5	5		
U12	VCCIO5	5			U12	VCCIO5	5		
V12	VCCIO5	5			V12	VCCIO5	5		
Y9	VCCIO5	5			Y9	VCCIO5	5		
AA4	VCCIO6	6			AA4	VCCIO6	6		
R10	VCCIO6	6			R10	VCCIO6	6		
R9	VCCIO6	6			R9	VCCIO6	6		
T4	VCCIO6	6			T4	VCCIO6	6		
V7	VCCIO6	6			V7	VCCIO6	6		
F4	VCCIO7	7			F4	VCCIO7	7		
J7	VCCIO7	7			J7	VCCIO7	7		
L4	VCCIO7	7			L4	VCCIO7	7		
M10	VCCIO7	7			M10	VCCIO7	7		
M9	VCCIO7	7			M9	VCCIO7	7		
AE25	VCCIO8	8			AE25	VCCIO8	8		
V18	VCCIO8	8			V18	VCCIO8	8		
J10	VCCAUX	-			J10	VCCAUX	-		
J11	VCCAUX	-			J11	VCCAUX	-		
J16	VCCAUX	-			J16	VCCAUX	-		
J17	VCCAUX	-			J17	VCCAUX	-		
K18	VCCAUX	-			K18	VCCAUX	-		
K9	VCCAUX	-			K9	VCCAUX	-		
L18	VCCAUX	-			L18	VCCAUX	-		
L9	VCCAUX	-			L9	VCCAUX	-		
T18	VCCAUX	-			T18	VCCAUX	-		
T9	VCCAUX	-			T9	VCCAUX	-		
U18	VCCAUX	-			U18	VCCAUX	-		
U9	VCCAUX	-			U9	VCCAUX	-		
V10	VCCAUX	-			V10	VCCAUX	-		
V11	VCCAUX	-			V11	VCCAUX	-		
V16	VCCAUX	-			V16	VCCAUX	-		
V17	VCCAUX	-			V17	VCCAUX	-		
A2	GND	-			A2	GND	-		
A25	GND	-			A25	GND	-		
AA18	GND	-			AA18	GND	-		
AA24	GND	-			AA24	GND	-		
AA3	GND	-			AA3	GND	-		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
AA9	GND	-			AA9	GND	-		
AD11	GND	-			AD11	GND	-		
AD16	GND	-			AD16	GND	-		
AD21	GND	-			AD21	GND	-		
AD6	GND	-			AD6	GND	-		
AE1	GND	-			AE1	GND	-		
AE26	GND	-			AE26	GND	-		
AF2	GND	-			AF2	GND	-		
AF25	GND	-			AF25	GND	-		
B1	GND	-			B1	GND	-		
B26	GND	-			B26	GND	-		
C11	GND	-			C11	GND	-		
C16	GND	-			C16	GND	-		
C21	GND	-			C21	GND	-		
C6	GND	-			C6	GND	-		
F18	GND	-			F18	GND	-		
F24	GND	-			F24	GND	-		
F3	GND	-			F3	GND	-		
F9	GND	-			F9	GND	-		
J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-		
J21	GND	-			J21	GND	-		
J6	GND	-			J6	GND	-		
K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-		
K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-		
K16	GND	-			K16	GND	-		
K17	GND	-			K17	GND	-		
L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-		
L16	GND	-			L16	GND	-		
L17	GND	-			L17	GND	-		
L24	GND	-			L24	GND	-		
L3	GND	-			L3	GND	-		
M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-		
N10	GND	-			N10	GND	-		
N12	GND	-			N12	GND	-		
N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-		
N15	GND	-			N15	GND	-		
N17	GND	-			N17	GND	-		
P10	GND	-			P10	GND	-		

LFE2-50E/50SE and LFE2-70E/70SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/50SE					LFE2-70E/70SE				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-		
P15	GND	-			P15	GND	-		
P17	GND	-			P17	GND	-		
R13	GND	-			R13	GND	-		
R14	GND	-			R14	GND	-		
T10	GND	-			T10	GND	-		
T11	GND	-			T11	GND	-		
T16	GND	-			T16	GND	-		
T17	GND	-			T17	GND	-		
T24	GND	-			T24	GND	-		
T3	GND	-			T3	GND	-		
U10	GND	-			U10	GND	-		
U11	GND	-			U11	GND	-		
U13	GND	-			U13	GND	-		
U14	GND	-			U14	GND	-		
U16	GND	-			U16	GND	-		
U17	GND	-			U17	GND	-		
V13	GND	-			V13	GND	-		
V14	GND	-			V14	GND	-		
V21	GND	-			V21	GND	-		
V6	GND	-			V6	GND	-		
M3	NC	-			M3	NC	-		
N6	NC	-			P24	NC	-		
P24	NC	-			N6	NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA

Ball Number	Ball Function	Bank	Dual Function	Differential
F4	PL2A	7	VREF2_7	T (LVDS)*
F3	PL2B	7	VREF1_7	C (LVDS)*
H4	PL3A	7		T
G5	PL3B	7		C
GND	GNDIO	7		
D2	PL4A	7		T (LVDS)*
D1	PL4B	7		C (LVDS)*
E2	PL5A	7		T
E1	PL5B	7		C
GND	GNDIO	7		
F1	PL14A	7	LUM1_SPLLT_IN_A	T (LVDS)*
F2	PL14B	7	LUM1_SPLLC_IN_A	C (LVDS)*
G1	PL15A	7	LUM1_SPLLT_FB_A	T
G2	PL15B	7	LUM1_SPLLC_FB_A	C
GND	GNDIO	7		
H8	PL18A	7		T
H6	PL18B	7		C
G4	PL19A	7		T (LVDS)*
G3	PL19B	7		C (LVDS)*
H7	PL20A	7		T
H5	PL20B	7		C
GND	GNDIO	7		
H2	PL21A	7	LDQS21	T (LVDS)*
H1	PL21B	7		C (LVDS)*
J6	PL22A	7		T
J8	PL22B	7		C
J2	PL23A	7		T (LVDS)*
J1	PL23B	7		C (LVDS)*
J5	PL24A	7		T
GND	GNDIO	7		
J7	PL24B	7		C
J4	PL25A	7		T (LVDS)*
J3	PL25B	7		C (LVDS)*
K6	PL26A	7		T
K8	PL26B	7		C
K2	PL27A	7		T (LVDS)*
K1	PL27B	7		C (LVDS)*
K5	PL28A	7		T
K7	PL28B	7		C
GND	GNDIO	7		
K4	PL29A	7	LDQS29	T (LVDS)*
K3	PL29B	7		C (LVDS)*
L8	PL30A	7		T

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
L6	PL30B	7		C
L2	PL31A	7		T (LVDS)*
L1	PL31B	7		C (LVDS)*
L7	PL32A	7		T
GND	GNDIO	7		
L5	PL32B	7		C
L4	PL33A	7		T (LVDS)*
L3	PL33B	7		C (LVDS)*
M8	PL34A	7		T
M6	PL34B	7		C
M2	PL35A	7		T (LVDS)*
M1	PL35B	7		C (LVDS)*
M7	PL36A	7		T
M5	PL36B	7		C
GND	GNDIO	7		
M4	PL37A	7	LDQS37	T (LVDS)*
M3	PL37B	7		C (LVDS)*
N6	PL38A	7	LUM0_SPLLT_IN_A	T
N8	PL38B	7	LUM0_SPLLC_IN_A	C
N5	PL39A	7	LUM0_SPLLT_FB_A	T
N7	PL39B	7	LUM0_SPLLC_FB_A	C
GND	GNDIO	7		
T9	PL50A	7		
R9	PL51A	7		T
P7	PL51B	7		C
N2	PL52A	7		T (LVDS)*
N1	PL52B	7		C (LVDS)*
P6	PL53A	7		T
P5	PL53B	7		C
GND	GNDIO	7		
P4	PL54A	7	LDQS54	T (LVDS)*
P3	PL54B	7		C (LVDS)*
R6	PL55A	7		T
R8	PL55B	7		C
P2	PL56A	7		T (LVDS)*
P1	PL56B	7		C (LVDS)*
R5	PL57A	7	PCLKT7_0	T
GND	GNDIO	7		
R7	PL57B	7	PCLKC7_0	C
R4	PL59A	6	PCLKT6_0	T (LVDS)*
R3	PL59B	6	PCLKC6_0	C (LVDS)*
T5	PL60A	6	VREF2_6	T
T7	PL60B	6	VREF1_6	C
T3	PL61A	6		T (LVDS)*

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
T4	PL61B	6		C (LVDS)*
T6	PL62A	6		T
T8	PL62B	6		C
T2	PL63A	6	LDQS63	T (LVDS)*
GND	GNDIO	6		
T1	PL63B	6		C (LVDS)*
U7	PL64A	6		T
U5	PL64B	6		C
U4	PL65A	6		T (LVDS)*
U3	PL65B	6		C (LVDS)*
U8	PL66A	6		T
U6	PL66B	6		C
GND	GNDIO	6		
U2	PL67A	6		T (LVDS)*
U1	PL67B	6		C (LVDS)*
V7	PL68A	6		T
V5	PL68B	6		C
V2	PL69A	6		T (LVDS)*
V1	PL69B	6		C (LVDS)*
V8	PL70A	6		T
V6	PL70B	6		C
GND	GNDIO	6		
W1	PL71A	6	LDQS71	T (LVDS)*
W2	PL71B	6		C (LVDS)*
W5	PL72A	6		T
W7	PL72B	6		C
W4	PL73A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
W3	PL73B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
W6	PL74A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO	6		
W8	PL74B	6	LLM0_GDLLC_FB_D	C
Y8	LLM0_PLLCAP	6		
Y1	PL76A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
Y2	PL76B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
Y5	PL77A	6	LLM0_GPLLT_FB_A	T
Y6	PL77B	6	LLM0_GPLLC_FB_A	C
Y4	PL78A	6		T (LVDS)*
Y3	PL78B	6		C (LVDS)*
AA6	PL79A	6		T
AA8	PL79B	6		C
AA2	PL80A	6	LDQS80	T (LVDS)*
GND	GNDIO	6		
AA1	PL80B	6		C (LVDS)*
AA7	PL81A	6		T

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AA5	PL81B	6		C
AA4	PL82A	6		T (LVDS)*
AA3	PL82B	6		C (LVDS)*
AB7	PL83A	6		T
AB5	PL83B	6		C
GND	GNDIO	6		
AB2	PL84A	6		T (LVDS)*
AB1	PL84B	6		C (LVDS)*
AB8	PL85A	6		T
AB6	PL85B	6		C
AB4	PL86A	6		T (LVDS)*
AB3	PL86B	6		C (LVDS)*
AC7	PL87A	6		T
AC5	PL87B	6		C
GND	GNDIO	6		
AC2	PL88A	6	LDQS88	T (LVDS)*
AC1	PL88B	6		C (LVDS)*
AC6	PL89A	6		T
AD6	PL89B	6		C
AD1	PL90A	6		T (LVDS)*
AD2	PL90B	6		C (LVDS)*
AD7	PL91A	6		T
GND	GNDIO	6		
AB9	PL91B	6		C
AD5	TCK	-		
AE7	TDI	-		
AD4	TMS	-		
AA9	TDO	-		
AD3	VCCJ	-		
AC8	PB2A	5	VREF2_5	T
AE8	PB2B	5	VREF1_5	C
AD8	PB3A	5		T
AF8	PB3B	5		C
AG7	PB4A	5		T
AH7	PB4B	5		C
AC9	PB5A	5		T
AE9	PB5B	5		C
AD9	PB6A	5	BDQS6	T
GND	GNDIO	5		
AF9	PB6B	5		C
AB10	PB7A	5		T
AA10	PB7B	5		C
AJ7	PB8A	5		T
AK7	PB8B	5		C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AC10	PB9A	5		T
AE10	PB9B	5		C
AJ8	PB10A	5		T
GND	GNDIO	5		
AK8	PB10B	5		C
AF6	PB11A	5		T
AF7	PB11B	5		C
AG5	PB12A	5		T
AH5	PB12B	5		C
AG6	PB13A	5		T
AH6	PB13B	5		C
AJ4	PB14A	5		T
AK4	PB14B	5		C
GND	GNDIO	5		
AJ5	PB15A	5	BDQS15	T
AK5	PB15B	5		C
AJ6	PB16A	5		T
AK6	PB16B	5		C
GND	GNDIO	5		
AD10	PB29A	5		T
AF10	PB29B	5		C
AC11	PB30A	5		T
AD11	PB30B	5		C
AG9	PB31A	5		T
AH9	PB31B	5		C
AE11	PB32A	5		T
AG10	PB32B	5		C
GND	GNDIO	5		
AJ9	PB33A	5	BDQS33	T
AK9	PB33B	5		C
AF11	PB34A	5		T
AH10	PB34B	5		C
AC12	PB35A	5		T
AE12	PB35B	5		C
AD12	PB36A	5		T
AF12	PB36B	5		C
AJ10	PB37A	5		T
AK10	PB37B	5		C
GND	GNDIO	5		
AG11	PB38A	5		T
AH11	PB38B	5		C
AE13	PB39A	5		T
AC13	PB39B	5		C
AF13	PB40A	5		T

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AD13	PB40B	5		C
AJ11	PB41A	5		T
AK11	PB41B	5		C
AD14	PB42A	5	BDQS42	T
GND	GNDIO	5		
AC14	PB42B	5		C
AG12	PB43A	5		T
AE14	PB43B	5		C
AJ12	PB44A	5		T
AK12	PB44B	5		C
AH12	PB45A	5		T
AF14	PB45B	5		C
AJ13	PB46A	5		T
GND	GNDIO	5		
AK13	PB46B	5		C
AB15	PB47A	5		T
AD15	PB47B	5		C
AE15	PB48A	5		T
AF15	PB48B	5		C
AG15	PB49A	5		T
AG14	PB49B	5		C
AH15	PB50A	5		T
AH14	PB50B	5		C
GND	GNDIO	5		
AJ14	PB51A	5	BDQS51	T
AK14	PB51B	5		C
AD16	PB52A	5		T
AF16	PB52B	5		C
AJ15	PB53A	5	PCLKT5_0	T
AK15	PB53B	5	PCLKC5_0	C
GND	GNDIO	5		
AE16	PB58A	4	PCLKT4_0	T
AC15	PB58B	4	PCLKC4_0	C
AJ16	PB59A	4		T
AK16	PB59B	4		C
AC16	PB60A	4	BDQS60	T
GND	GNDIO	4		
AB16	PB60B	4		C
AH17	PB61A	4		T
AG17	PB61B	4		C
AF17	PB62A	4		T
AD17	PB62B	4		C
AE17	PB63A	4		T
AC17	PB63B	4		C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AJ17	PB64A	4		T
GND	GNDIO	4		
AK17	PB64B	4		C
AK18	PB65A	4		T
AJ18	PB65B	4		C
AD18	PB66A	4		T
AF18	PB66B	4		C
AC18	PB67A	4		T
AE18	PB67B	4		C
AG19	PB68A	4		T
AH19	PB68B	4		C
GND	GNDIO	4		
AE19	PB69A	4	BDQS69	T
AF19	PB69B	4		C
AC19	PB70A	4		T
AD19	PB70B	4		C
AJ19	PB71A	4		T
AK19	PB71B	4		C
AF20	PB72A	4		T
AH20	PB72B	4		C
AE20	PB73A	4		T
AG20	PB73B	4		C
GND	GNDIO	4		
AD20	PB74A	4		T
AC20	PB74B	4		C
AH21	PB75A	4		T
AF21	PB75B	4		C
AJ20	PB76A	4		T
AK20	PB76B	4		C
AG21	PB77A	4		T
AE21	PB77B	4		C
AD21	PB78A	4	BDQS78	T
GND	GNDIO	4		
AC21	PB78B	4		C
AD22	PB79A	4		T
AB21	PB79B	4		C
AJ21	PB80A	4		T
AK21	PB80B	4		C
GND	GNDIO	4		
AJ25	PB87A	4	BDQS87	T
AK24	PB87B	4		C
AJ24	PB88A	4		T
AK25	PB88B	4		C
AH24	PB89A	4		T

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AH25	PB89B	4		C
AJ26	PB90A	4		T
AK26	PB90B	4		C
AF25	PB91A	4		T
AG25	PB91B	4		C
GND	GNDIO	4		
AK22	PB92A	4		T
AJ22	PB92B	4		C
AE22	PB93A	4		T
AF22	PB93B	4		C
AG22	PB94A	4		T
AH22	PB94B	4		C
AG24	PB95A	4		T
AG23	PB95B	4		C
AE23	PB96A	4	BDQS96	
GND	GNDIO	4		
AC22	PB97A	4		
AJ23	PB98A	4		T
AK23	PB98B	4		C
AD24	PB99A	4		T
AF24	PB99B	4		C
AC23	PB100A	4	VREF2_4	T
GND	GNDIO	4		
AE24	PB100B	4	VREF1_4	C
AE25	CFG2	8		
AB22	CFG1	8		
AE26	CFG0	8		
AA22	PROGRAMN	8		
AD25	CCLK	8		
AD26	INITN	8		
AC24	DONE	8		
GND	GNDIO	4		
AC25	PR90B	8	WRITEN	C
AE27	PR90A	8	CS1N	T
AC26	PR89B	8	CSN	C
AE28	PR89A	8	D0	T
AD27	PR88B	8	D1	C
AD28	PR88A	8	D2	T
AB24	PR87B	8	D3	C
GND	GNDIO	4		
AB23	PR87A	8	D4	T
AB25	PR86B	8	D5	C
AB26	PR86A	8	D6	T
AC27	PR85B	8	D7	C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AB27	PR85A	8	DI/CSSPI0N	T
AD29	PR84B	8	DOUT/CSON	C
AD30	PR84A	8	BUSY/SISPI	T
AA25	PR83B	3		C
GND	GNDIO	3		
AA23	PR83A	3		T
AC29	PR82B	3		C (LVDS)*
AC30	PR82A	3		T (LVDS)*
AA26	PR81B	3		C
AA24	PR81A	3		T
AB29	PR80B	3		C (LVDS)*
AB30	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO	3		
Y23	PR79B	3		C
Y25	PR79A	3		T
AA27	PR78B	3		C (LVDS)*
AA28	PR78A	3		T (LVDS)*
Y24	PR77B	3	RLM0_GPLLC_FB_A	C
Y26	PR77A	3	RLM0_GPLLT_FB_A	T
AA29	PR76B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
AA30	PR76A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
R22	RLM0_PLLCAP	3		
W23	PR74B	3	RLM0_GDLLC_FB_A	C
W25	PR74A	3	RLM0_GDLLT_FB_A	T
GND	GNDIO	3		
Y27	PR73B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
Y28	PR73A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
W24	PR72B	3		C
W26	PR72A	3		T
Y29	PR71B	3		C (LVDS)*
Y30	PR71A	3	RDQS71	T (LVDS)*
V25	PR70B	3		C
GND	GNDIO	3		
V23	PR70A	3		T
W27	PR69B	3		C (LVDS)*
W28	PR69A	3		T (LVDS)*
V26	PR68B	3		C
V24	PR68A	3		T
W29	PR67B	3		C (LVDS)*
W30	PR67A	3		T (LVDS)*
U25	PR66B	3		C
GND	GNDIO	3		
U23	PR66A	3		T
V29	PR65B	3		C (LVDS)*

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
V30	PR65A	3		T (LVDS)*
U26	PR64B	3		C
U24	PR64A	3		T
U27	PR63B	3		C (LVDS)*
U28	PR63A	3	RDQS63	T (LVDS)*
GND	GNDIO	3		
T23	PR62B	3		C
T25	PR62A	3		T
U29	PR61B	3		C (LVDS)*
U30	PR61A	3		T (LVDS)*
T24	PR60B	3	VREF2_3	C
T26	PR60A	3	VREF1_3	T
T27	PR59B	3	PCLKC3_0	C (LVDS)*
T28	PR59A	3	PCLKT3_0	T (LVDS)*
R24	PR57B	2	PCLKC2_0	C
R26	PR57A	2	PCLKT2_0	T
GND	GNDIO	2		
T29	PR56B	2		C (LVDS)*
T30	PR56A	2		T (LVDS)*
R23	PR55B	2		C
R25	PR55A	2		T
R27	PR54B	2		C (LVDS)*
R28	PR54A	2	RDQS54	T (LVDS)*
P26	PR53B	2		C
GND	GNDIO	2		
P24	PR53A	2		T
R29	PR52B	2		C (LVDS)*
R30	PR52A	2		T (LVDS)*
P25	PR51B	2		C
P23	PR51A	2		T
P27	PR50B	2		C (LVDS)*
P28	PR50A	2		T (LVDS)*
GND	GNDIO	2		
N24	PR39B	2	RUM0_SPLLC_FB_A	C
N26	PR39A	2	RUM0_SPLLT_FB_A	T
N23	PR38B	2	RUM0_SPLLC_IN_A	C
N25	PR38A	2	RUM0_SPLLT_IN_A	T
P29	PR37B	2		C (LVDS)*
P30	PR37A	2	RDQS37	T (LVDS)*
M26	PR36B	2		C
GND	GNDIO	2		
M24	PR36A	2		T
N29	PR35B	2		C (LVDS)*
N30	PR35A	2		T (LVDS)*

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
M25	PR34B	2		C
M23	PR34A	2		T
M27	PR33B	2		C (LVDS)*
M28	PR33A	2		T (LVDS)*
L26	PR32B	2		C
GND	GNDIO	2		
L24	PR32A	2		T
M29	PR31B	2		C (LVDS)*
M30	PR31A	2		T (LVDS)*
L25	PR30B	2		C
L23	PR30A	2		T
L27	PR29B	2		C (LVDS)*
L28	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO	2		
K24	PR28B	2		C
K26	PR28A	2		T
L29	PR27B	2		C (LVDS)*
L30	PR27A	2		T (LVDS)*
K23	PR26B	2		C
K25	PR26A	2		T
K27	PR25B	2		C (LVDS)*
K28	PR25A	2		T (LVDS)*
J24	PR24B	2		C
J26	PR24A	2		T
GND	GNDIO	2		
K29	PR23B	2		C (LVDS)*
K30	PR23A	2		T (LVDS)*
J23	PR22B	2		C
J25	PR22A	2		T
J27	PR21B	2		C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2		C
GND	GNDIO	2		
H24	PR20A	2		T
J29	PR19B	2		C (LVDS)*
J30	PR19A	2		T (LVDS)*
H25	PR18B	2		C
H23	PR18A	2		T
G27	PR15B	2	RUM1_SPLLC_FB_A	C
GND	GNDIO	2		
H27	PR15A	2	RUM1_SPLLT_FB_A	T
G29	PR14B	2	RUM1_SPLLC_IN_A	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A	T (LVDS)*
GND	GNDIO	2		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO	2		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO	1		
C25	PT99B	1		C
D25	PT99A	1		T
J22	PT98B	1		C
J21	PT98A	1		T
B25	PT97B	1		C
A25	PT97A	1		T
E24	PT96B	1		C
F24	PT96A	1		T
GND	GNDIO	1		
F23	PT95B	1		C
H22	PT95A	1		T
D24	PT94B	1		C
C24	PT94A	1		T
E23	PT93B	1		C
G23	PT93A	1		T
B24	PT92B	1		C
A24	PT92A	1		T
C27	PT91B	1		C
GND	GNDIO	1		
D27	PT91A	1		T
C26	PT90B	1		C
D26	PT90A	1		T
A27	PT89B	1		C
B27	PT89A	1		T
A28	PT88B	1		C
B28	PT88A	1		T
A29	PT87B	1		C
B29	PT87A	1		T
GND	GNDIO	1		
H21	PT80B	1		C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
F22	PT80A	1		T
B23	PT79B	1		C
A23	PT79A	1		T
G24	PT78B	1		C
E22	PT78A	1		T
GND	GNDIO	1		
D22	PT77B	1		C
C22	PT77A	1		T
G22	PT76B	1		C
E21	PT76A	1		T
B22	PT75B	1		C
A22	PT75A	1		T
H20	PT74B	1		C
F21	PT74A	1		T
F20	PT73B	1		C
GND	GNDIO	1		
H19	PT73A	1		T
D21	PT72B	1		C
C21	PT72A	1		T
E20	PT71B	1		C
G21	PT71A	1		T
B21	PT70B	1		C
A21	PT70A	1		T
F19	PT69B	1		C
G20	PT69A	1		T
E19	PT68B	1		C
GND	GNDIO	1		
G19	PT68A	1		T
D20	PT67B	1		C
C20	PT67A	1		T
B20	PT66B	1		C
A20	PT66A	1		T
F18	PT65B	1		C
H18	PT65A	1		T
D19	PT64B	1		C
C19	PT64A	1		T
GND	GNDIO	1		
G18	PT63B	1		C
E18	PT63A	1		T
H17	PT62B	1		C
F17	PT62A	1		T
G17	PT61B	1		C
E17	PT61A	1		T
B19	PT60B	1		C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
A19	PT60A	1		T
GND	GNDIO	1		
D17	PT59B	1		C
B18	PT59A	1		T
C17	PT58B	1		C
A18	PT58A	1		T
H16	PT57B	1	PCLKC1_0	C
F16	PT57A	1	PCLKT1_0	T
K16	XRES	1		
E16	PT55B	0	PCLKC0_0	C
GND	GNDIO	0		
G16	PT55A	0	PCLKT0_0	T
B17	PT54B	0		C
A17	PT54A	0		T
J15	PT53B	0		C
J16	PT53A	0		T
C16	PT52B	0		C
D16	PT52A	0		T
F15	PT51B	0		C
H15	PT51A	0		T
E15	PT50B	0		C
GND	GNDIO	0		
G15	PT50A	0		T
C15	PT49B	0		C
D15	PT49A	0		T
B16	PT48B	0		C
A16	PT48A	0		T
E14	PT47B	0		C
G14	PT47A	0		T
B15	PT46B	0		C
A15	PT46A	0		T
GND	GNDIO	0		
H14	PT45B	0		C
F14	PT45A	0		T
D14	PT44B	0		C
C14	PT44A	0		T
G13	PT43B	0		C
E13	PT43A	0		T
B14	PT42B	0		C
A14	PT42A	0		T
GND	GNDIO	0		
H13	PT41B	0		C
F13	PT41A	0		T
G12	PT40B	0		C

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
E12	PT40A	0		T
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO	0		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO	0		
A11	PT32A	0		T
E10	PT31B	0		C
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO	0		
D7	PT14A	0		T
D8	PT13B	0		C
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T
C5	PT11B	0		C
D5	PT11A	0		T
E9	PT10B	0		C
G9	PT10A	0		T
GND	GNDIO	0		
B10	PT9B	0		C
A10	PT9A	0		T

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
D9	PT8B	0		C
C9	PT8A	0		T
F9	PT7B	0		C
H9	PT7A	0		T
B9	PT6B	0		C
A9	PT6A	0		T
GND	GNDIO	0		
E8	PT5B	0		C
G8	PT5A	0		T
A8	PT4B	0		C
B8	PT4A	0		T
F8	PT3B	0		C
F7	PT3A	0		T
J10	PT2B	0	VREF2_0	C
J9	PT2A	0	VREF1_0	T
AA11	VCC	-		
AA20	VCC	-		
K11	VCC	-		
K21	VCC	-		
K22	VCC	-		
L11	VCC	-		
L12	VCC	-		
L13	VCC	-		
L18	VCC	-		
L19	VCC	-		
L20	VCC	-		
M11	VCC	-		
M20	VCC	-		
N11	VCC	-		
N20	VCC	-		
V11	VCC	-		
V20	VCC	-		
W11	VCC	-		
W20	VCC	-		
Y10	VCC	-		
Y11	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
Y20	VCC	-		
J13	VCCIO0	0		
J14	VCCIO0	0		
K12	VCCIO0	0		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
K13	VCCIO0	0		
K14	VCCIO0	0		
K15	VCCIO0	0		
J17	VCCIO1	1		
J18	VCCIO1	1		
J20	VCCIO1	1		
K17	VCCIO1	1		
K18	VCCIO1	1		
K20	VCCIO1	1		
L21	VCCIO2	2		
M21	VCCIO2	2		
M22	VCCIO2	2		
N21	VCCIO2	2		
N22	VCCIO2	2		
R21	VCCIO2	2		
U21	VCCIO3	3		
U22	VCCIO3	3		
V21	VCCIO3	3		
V22	VCCIO3	3		
W21	VCCIO3	3		
Y22	VCCIO3	3		
AA16	VCCIO4	4		
AA17	VCCIO4	4		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AB17	VCCIO4	4		
AB18	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AA14	VCCIO5	5		
AB12	VCCIO5	5		
AB13	VCCIO5	5		
AB14	VCCIO5	5		
U10	VCCIO6	6		
U9	VCCIO6	6		
V10	VCCIO6	6		
W10	VCCIO6	6		
W9	VCCIO6	6		
Y9	VCCIO6	6		
L10	VCCIO7	7		
L9	VCCIO7	7		
M10	VCCIO7	7		
N10	VCCIO7	7		
P10	VCCIO7	7		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
R10	VCCIO7	7		
AA21	VCCIO8	8		
Y21	VCCIO8	8		
AA15	VCCAUX	-		
AB11	VCCAUX	-		
AB19	VCCAUX	-		
AB20	VCCAUX	-		
J11	VCCAUX	-		
J12	VCCAUX	-		
J19	VCCAUX	-		
K19	VCCAUX	-		
L22	VCCAUX	-		
M9	VCCAUX	-		
N9	VCCAUX	-		
P21	VCCAUX	-		
P9	VCCAUX	-		
T10	VCCAUX	-		
T21	VCCAUX	-		
V9	VCCAUX	-		
W22	VCCAUX	-		
A1	GND	-		
A30	GND	-		
AC28	GND	-		
AC3	GND	-		
AH13	GND	-		
AH18	GND	-		
AH23	GND	-		
AH28	GND	-		
AH3	GND	-		
AH8	GND	-		
AK1	GND	-		
AK30	GND	-		
C13	GND	-		
C18	GND	-		
C23	GND	-		
C28	GND	-		
C3	GND	-		
C8	GND	-		
H28	GND	-		
H3	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
M12	GND	-		
M13	GND	-		
M14	GND	-		
M15	GND	-		
M16	GND	-		
M17	GND	-		
M18	GND	-		
M19	GND	-		
N12	GND	-		
N13	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N18	GND	-		
N19	GND	-		
N28	GND	-		
N3	GND	-		
P11	GND	-		
P12	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P19	GND	-		
P20	GND	-		
R11	GND	-		
R12	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R19	GND	-		
R20	GND	-		
T11	GND	-		
T12	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
T17	GND	-		
T18	GND	-		
T19	GND	-		
T20	GND	-		
U11	GND	-		
U12	GND	-		
U13	GND	-		
U14	GND	-		
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U19	GND	-		
U20	GND	-		
V12	GND	-		
V13	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V18	GND	-		
V19	GND	-		
V28	GND	-		
V3	GND	-		
W12	GND	-		
W13	GND	-		
W14	GND	-		
W15	GND	-		
W16	GND	-		
W17	GND	-		
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		
AG4	NC	-		
AG8	NC	-		
AH1	NC	-		
AH16	NC	-		
AH2	NC	-		
AH26	NC	-		
AH27	NC	-		
AH29	NC	-		
AH30	NC	-		
AH4	NC	-		
AJ1	NC	-		
AJ2	NC	-		
AJ27	NC	-		
AJ28	NC	-		
AJ29	NC	-		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AJ3	NC	-		
AJ30	NC	-		
AK2	NC	-		
AK27	NC	-		
AK28	NC	-		
AK29	NC	-		
AK3	NC	-		
B1	NC	-		
B2	NC	-		
B3	NC	-		
B30	NC	-		
B4	NC	-		
B5	NC	-		
C1	NC	-		
C2	NC	-		
C29	NC	-		
C30	NC	-		
C4	NC	-		
D13	NC	-		
D18	NC	-		
D23	NC	-		
D28	NC	-		
D29	NC	-		
D3	NC	-		
D30	NC	-		
D4	NC	-		
E25	NC	-		
E26	NC	-		
E27	NC	-		
E28	NC	-		
E29	NC	-		
E3	NC	-		
E30	NC	-		
E4	NC	-		
E5	NC	-		
E6	NC	-		
F25	NC	-		
F5	NC	-		
F6	NC	-		
G6	NC	-		
G7	NC	-		
K10	NC	-		
K9	NC	-		
N27	NC	-		

LFE2-70E/70SE Logic Signal Connections: 900 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
N4	NC	-		
R1	NC	-		
R2	NC	-		
V27	NC	-		
V4	NC	-		
P22	VCCPLL	-		
P8	VCCPLL	-		
T22	VCCPLL	-		
Y7	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
A2	PL2A	7		T (LVDS)*	PL2A	7		T (LVDS)*
B2	PL2B	7		C (LVDS)*	PL2B	7		C(LVDS)*
D3	PL3A	7		T	PL3A	7		T
C2	PL3B	7		C	PL3B	7		C
E4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
E5	PL4B	7		C (LVDS)*	PL4B	7		C(LVDS)*
B1	PL5A	7		T	PL5A	7		T
C1	PL5B	7		C	PL5B	7		C
D2	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	7			GNDIO7	7		
D1	PL6B	7		C (LVDS)*	PL6B	7		C(LVDS)*
E1	PL7A	7		T	PL7A	7		T
F1	PL7B	7		C	PL7B	7		C
VCCIO	VCCIO7	7			VCCIO7	7		
F3	PL8A	7		T (LVDS)*	PL8A	7		T (LVDS)*
F2	PL8B	7		C (LVDS)*	PL8B	7		C(LVDS)*
F6	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F5	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	7			GNDIO7	7		
G4	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
G3	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A	C(LVDS)*
G1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A	T
G2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A	C
H1	PL13A	7		T (LVDS)*	PL13A	7		T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
J1	PL13B	7		C (LVDS)*	PL13B	7		C(LVDS)*
H2	PL14A	7		T	PL14A	7		T
H3	PL14B	7		C	PL14B	7		C
GNDIO	GNDIO7	7			GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
G6	PL24A	7		T (LVDS)*	PL34A	7		T (LVDS)*
H6	PL24B	7		C (LVDS)*	PL34B	7		C(LVDS)*
J2	PL25A	7	PCLKT7_0	T	PL35A	7	PCLKT7_0	T
GNDIO	GNDIO7	7			GNDIO7	7		
K1	PL25B	7	PCLKC7_0	C	PL35B	7	PCLKC7_0	C
H4	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*
H5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C(LVDS)*
J4	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T
K4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C
VCCIO	VCCIO6	6			VCCIO6	6		
J6	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	6			GNDIO6	6		
J5	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C(LVDS)*
K3	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T
K2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	6			GNDIO6	6		

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
L1	PL42A	6	LLM0_GPLLT_IN_A	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57	T (LVDS)*
GNDIO	GNDIO6	6			GNDIO6	6		
L2	PL42B	6	LLM0_GPLLC_IN_A	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**	C(LVDS)*
L3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A	T
L4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
M1	PL44A	6	LLM0_GDLLT_IN_A	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
N1	PL44B	6	LLM0_GDLLC_IN_A	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**	C(LVDS)*
N2	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A	T
N3	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	6			GNDIO6	6		
M4	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	6			GNDIO6	6		
K6	TCK	-			TCK	-		
L5	TDI	-			TDI	-		
N4	TMS	-			TMS	-		
N6	TDO	-			TDO	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5		T	PB2A	5		T
N5	PB2B	5		C	PB2B	5		C
L6	PB3A	5		T	PB3A	5		T
M6	PB3B	5		C	PB3B	5		C
P3	PB4A	5		T	PB4A	5		T
VCCIO	VCCIO5	5			VCCIO5	5		
P4	PB4B	5		C	PB4B	5		C
P2	PB5A	5		T	PB5A	5		T
P1	PB5B	5		C	PB5B	5		C
R1	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	5			GNDIO5	5		
R2	PB6B	5		C	PB6B	5		C
R3	PB7A	5		T	PB7A	5		T
T2	PB7B	5		C	PB7B	5		C
R4	PB8A	5		T	PB8A	5		T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB8B	5		C	PB8B	5		C
T4	PB10A	5		T	PB10A	5		T
GNDIO	GNDIO5	5			GNDIO5	5		
T5	PB10B	5		C	PB10B	5		C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	5			GNDIO5	5		
T6	PB16A	5	VREF2_5	T	PB34A	5	VREF2_5	T
R6	PB16B	5	VREF1_5	C	PB34B	5	VREF1_5	C
P6	PB17A	5	PCLKT5_0	T	PB35A	5	PCLKT5_0	T
P7	PB17B	5	PCLKC5_0	C	PB35B	5	PCLKC5_0	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	5			GNDIO5	5		
T7	PB22A	4	PCLKT4_0	T	PB40A	4	PCLKT4_0	T

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO4	4			VCCIO4	4		
T8	PB22B	4	PCLKC4_0	C	PB40B	4	PCLKC4_0	C
L7	PB23A	4	VREF2_4	T	PB41A	4	VREF2_4	T
L8	PB23B	4	VREF1_4	C	PB41B	4	VREF1_4	C
GNDIO	GNDIO4	4			GNDIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	4			GNDIO4	4		
P8	PB29A	4		T	PB47A	4		T
N8	PB29B	4		C	PB47B	4		C
R7	PB30A	4		T	PB48A	4		T
R8	PB30B	4		C	PB48B	4		C
N7	PB31A	4		T	PB49A	4		T
M8	PB31B	4		C	PB49B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
R9	PB32A	4		T	PB50A	4		T
T9	PB32B	4		C	PB50B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
T10	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T
R10	PB33B	4		C	PB51B	4		C
N9	PB34A	4		T	PB52A	4		T
P10	PB34B	4		C	PB52B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	4			GNDIO4	4		
L9	PB47A	4		T	PB65A	4		T
M9	PB47B	4		C	PB65B	4		C
T11	PB49A	4		T	PB67A	4		T
R11	PB49B	4		C	PB67B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
T12	PB50A	4		T	PB68A	4		T
T13	PB50B	4		C	PB68B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
P11	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T
N10	PB51B	4		C	PB69B	4		C
T14	PB52A	4		T	PB70A	4		T
R13	PB52B	4		C	PB70B	4		C
R15	PB53A	4		T	PB71A	4		T
R16	PB53B	4		C	PB71B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
R14	PB54A	4		T	PB72A	4		T
P15	PB54B	4		C	PB72B	4		C
P16	PB55A	4		T	PB73A	4		T
P14	PB55B	4		C	PB73B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
L11	CFG2	8			CFG2	8		
L10	CFG1	8			CFG1	8		
P13	CFG0	8			CFG0	8		
N12	PROGRAMN	8			PROGRAMN	8		
N11	CCLK	8			CCLK	8		

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
M11	INITN	8			INITN	8		
N13	DONE	8			DONE	8		
GNDIO	GNDIO8	8			GNDIO8	8		
M12	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
M13	PR53A	8	CS1N	T	PR68A	8	CS1N	T
N14	PR52B	8	CSN	C	PR67B	8	CSN	C
N15	PR52A	8	D0	T	PR67A	8	D0	T
VCCIO	VCCIO8	8			VCCIO8	8		
N16	PR51B	8	D1	C	PR66B	8	D1	C
M16	PR51A	8	D2	T	PR66A	8	D2	T
L12	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	8			GNDIO8	8		
L13	PR50A	8	D4	T	PR65A	8	D4	T
L16	PR49B	8	D5	C	PR64B	8	D5	C
K16	PR49A	8	D6	T	PR64A	8	D6	T
L14	PR48B	8	D7	C	PR63B	8	D7	C
VCCIO	VCCIO8	8			VCCIO8	8		
L15	PR48A	8	DI	T	PR63A	8	DI	T
K13	PR47B	8	DOUT_CSON	C	PR62B	8	DOUT_CSON	C
K14	PR47A	8	BUSY	T	PR62A	8	BUSY	T
K11	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
K15	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	3			GNDIO3	3		
J16	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A	T
H16	PR44B	3	RLM0_GDLLC_IN_A	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**	C(LVDS)*
J15	PR44A	3	RLM0_GDLLT_IN_A	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
J14	PR43B	3	RLM0_GPLLC_IN_A	C	PR58B	3	RLM0_GPLLC_IN_A**	C
VCCIO	VCCIO3	3			VCCIO3	3		
J13	PR43A	3	RLM0_GPLLT_IN_A	T	PR58A	3	RLM0_GPLLT_IN_A**	T
H13	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A	C(LVDS)*
H12	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57	T (LVDS)*
GNDIO	GNDIO3	3			GNDIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
G16	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
H15	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
E16	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C(LVDS)*
F15	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	3			GNDIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
F16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
G15	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J11	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C(LVDS)*
J12	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
G14	PR25B	2	PCLKC2_0	C	PR35B	2	PCLKC2_0	C
G13	PR25A	2	PCLKT2_0	T	PR35A	2	PCLKT2_0	T
GNDIO	GNDIO2	2			GNDIO2	2		
F14	PR24B	2		C (LVDS)*	PR34B	2		C(LVDS)*

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
F13	PR24A	2		T (LVDS)*	PR34A	2		T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
GNDIO	GNDIO2	2			GNDIO2	2		
H11	PR14B	2		C	PR14B	2		C
G11	PR14A	2		T	PR14A	2		T
E13	PR13B	2		C (LVDS)*	PR13B	2		C(LVDS)*
F12	PR13A	2		T (LVDS)*	PR13A	2		T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A	C
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A	T
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A	C(LVDS)*
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	2			GNDIO2	2		
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			VCCIO2	2		
F4	XRES	-			XRES	-		
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	1			GNDIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO0	0			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
G10	VCCPLL	-			VCCPLL	-		
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
E7	VCCIO0	0			VCCIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
E10	VCCIO1	1			VCCIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
VCCIO	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
VCCIO	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
VCCIO	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
VCCIO	VCCIO8	8			VCCIO8	8		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A15	GND	-			GND	-		
A16	GND	-			GND	-		
A3	GND	-			GND	-		

LFE2M20E/20SE and LFE2M35E/35SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
A9	GND	-			GND	-		
B12	GND	-			GND	-		
B6	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		
R12	GND	-			GND	-		
R5	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
D10	NC	-			NC	-		
D11	NC	-			NC	-		
D12	NC	-			NC	-		
D13	NC	-			NC	-		
D14	NC	-			NC	-		
D4	NC	-			NC	-		
D5	NC	-			NC	-		
D6	NC	-			NC	-		
D7	NC	-			NC	-		
E11	NC	-			NC	-		
E6	NC	-			NC	-		
E8	NC	-			NC	-		
E9	NC	-			NC	-		
F10	NC	-			NC	-		
F7	NC	-			NC	-		
F8	NC	-			NC	-		
F9	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
D1	PL2A	7		T (LVDS)*	PL2A	7		T (LVDS)*
E1	PL2B	7		C (LVDS)*	PL2B	7		C (LVDS)*
F1	PL3A	7		T	PL3A	7		T
F2	PL3B	7		C	PL3B	7		C
F5	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
G6	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*
F4	PL5A	7		T	PL5A	7		T
F3	PL5B	7		C	PL5B	7		C
G1	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	7			GNDIO7	7		
G2	PL6B	7		C (LVDS)*	PL6B	7		C (LVDS)*
H1	PL7A	7		T	PL7A	7		T
H2	PL7B	7		C	PL7B	7		C
VCCIO	VCCIO7	7			VCCIO7	7		
H7	PL8A	7		T (LVDS)*	PL8A	7		T (LVDS)*
H6	PL8B	7		C (LVDS)*	PL8B	7		C (LVDS)*
G3	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
H3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	7			GNDIO7	7		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A	C
J3	PL13A	7		T (LVDS)*	PL13A	7		T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL13B	7		C (LVDS)*	PL13B	7		C (LVDS)*
J7	PL14A	7		T	PL14A	7		T
J6	PL14B	7		C	PL14B	7		C
GNDIO	GNDIO7	7			GNDIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
K1	PL18A	7	LUM1_SPLLT_IN_A	T (LVDS)*	PL28A	7	LUM1_SPLLT_IN_A	T (LVDS)*
K2	PL18B	7	LUM1_SPLLC_IN_A	C (LVDS)*	PL28B	7	LUM1_SPLLC_IN_A	C (LVDS)*
J5	PL19A	7	LUM1_SPLLT_FB_A	T	PL29A	7	LUM1_SPLLT_FB_A	T
K5	PL19B	7	LUM1_SPLLC_FB_A	C	PL29B	7	LUM1_SPLLC_FB_A	C
VCCIO	VCCIO7	7			VCCIO7	7		
K7	PL20A	7		T (LVDS)*	PL30A	7		T (LVDS)*
K6	PL20B	7		C (LVDS)*	PL30B	7		C (LVDS)*
L6	PL21A	7		T	PL31A	7		T
L7	PL21B	7		C	PL31B	7		C
GNDIO	GNDIO7	7			GNDIO7	7		
L1	PL22A	7	LDQS22	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*
L2	PL22B	7		C (LVDS)*	PL32B	7		C (LVDS)*
M7	PL23A	7		T	PL33A	7		T
VCCIO	VCCIO7	7			VCCIO7	7		
L5	PL23B	7		C	PL33B	7		C
L3	PL24A	7		T (LVDS)*	PL34A	7		T (LVDS)*
L4	PL24B	7		C (LVDS)*	PL34B	7		C (LVDS)*

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
M1	PL25A	7	PCLKT7_0	T	PL35A	7	PCLKT7_0	T
GNDIO	GNDIO7	7			GNDIO7	7		
M2	PL25B	7	PCLKC7_0	C	PL35B	7	PCLKC7_0	C
M6	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*
M5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*
M3	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T
M4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C
VCCIO	VCCIO6	6			VCCIO6	6		
N7	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	6			GNDIO6	6		
N6	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*
N1	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T
N2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	6			GNDIO6	6		
P6	PL38A	6	LDQS38	T (LVDS)*	PL48A	6	LDQS48	T (LVDS)*
N5	PL38B	6		C (LVDS)*	PL48B	6		C (LVDS)*
P1	PL39A	6		T	PL49A	6		T
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL39B	6		C	PL49B	6		C
P3	PL40A	6		T (LVDS)*	PL50A	6		T (LVDS)*
P4	PL40B	6		C (LVDS)*	PL50B	6		C (LVDS)*
P5	PL41A	6		T	PL51A	6		T
GNDIO	GNDIO6	6			GNDIO6	6		
P7	PL41B	6		C	PL51B	6		C
R1	PL42A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57	T (LVDS)*
GNDIO	GNDIO6	6			GNDIO6	6		
R2	PL42B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
R3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A	T
R4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
R6	PL44A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
R5	PL44B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
T1	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A	T
T2	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	6			GNDIO6	6		
R7	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
T6	PL47A	6		T (LVDS)*	PL62A	6		T (LVDS)*
T7	PL47B	6		C (LVDS)*	PL62B	6		C (LVDS)*
U1	PL48A	6		T	PL63A	6		T
U2	PL48B	6		C	PL63B	6		C
VCCIO	VCCIO6	6			VCCIO6	6		
T3	PL49A	6		T (LVDS)*	PL64A	6		T (LVDS)*
U3	PL49B	6		C (LVDS)*	PL64B	6		C (LVDS)*
U6	PL50A	6		T	NC	-		
U5	PL50B	6		C	PL65B	6		C
GNDIO	GNDIO6	6			GNDIO6	6		
V5	PL51A	6	LDQS51	T (LVDS)*	PL66A	6	LDQS66	T (LVDS)*

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
U4	PL51B	6		C (LVDS)*	PL66B	6		C (LVDS)*
V1	PL52A	6		T	PL67A	6		T
VCCIO	VCCIO6	6			VCCIO6	6		
V3	PL52B	6		C	PL67B	6		C
W1	PL53A	6		T (LVDS)*	PL68A	6		T (LVDS)*
Y1	PL53B	6		C (LVDS)*	PL68B	6		C (LVDS)*
AA1	PL54A	6		T	PL69A	6		T
GNDIO	GNDIO6	6			GNDIO6	6		
AA2	PL54B	6		C	PL69B	6		C
V4	TCK	-			TCK	-		
Y2	TDI	-			TDI	-		
Y3	TMS	-			TMS	-		
W3	TDO	-			TDO	-		
W4	VCCJ	-			VCCJ	-		
W5	PB2A	5		T	PB2A	5		T
Y4	PB2B	5		C	PB2B	5		C
W6	PB3A	5		T	PB3A	5		T
V6	PB3B	5		C	PB3B	5		C
AA3	PB4A	5		T	PB4A	5		T
VCCIO	VCCIO5	5			VCCIO5	5		
AB2	PB4B	5		C	PB4B	5		C
T8	PB5A	5		T	PB5A	5		T
U7	PB5B	5		C	PB5B	5		C
U8	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	5			GNDIO5	5		
T9	PB6B	5		C	PB6B	5		C
V8	PB7A	5		T	PB7A	5		T
W8	PB7B	5		C	PB7B	5		C
Y6	PB8A	5		T	PB8A	5		T
VCCIO	VCCIO5	5			VCCIO5	5		
Y5	PB8B	5		C	PB8B	5		C
AB3	PB9A	5		T	PB9A	5		T
AB4	PB9B	5		C	PB9B	5		C
AB5	PB10A	5		T	PB10A	5		T
GNDIO	GNDIO5	5			GNDIO5	5		
AA6	PB10B	5		C	PB10B	5		C
V9	PB13A	5		T	PB31A	5		T
U9	PB13B	5		C	PB31B	5		C
VCCIO	VCCIO5	5			VCCIO5	5		
-	-	-			GNDIO5	5		
U10	PB14A	5		T	PB32A	5		T
T10	PB14B	5		C	PB32B	5		C
GNDIO	GNDIO5	5			GNDIO5	5		
W9	PB15A	5	BDQS15	T	PB33A	5	BDQS33	T
Y8	PB15B	5		C	PB33B	5		C
AA7	PB16A	5	VREF2_5	T	PB34A	5	VREF2_5	T
Y7	PB16B	5	VREF1_5	C	PB34B	5	VREF1_5	C
AB6	PB17A	5	PCLKT5_0	T	PB35A	5	PCLKT5_0	T

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
AB7	PB17B	5	PCLKC5_0	C	PB35B	5	PCLKC5_0	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	5			GNDIO5	5		
AA8	PB22A	4	PCLKT4_0	T	PB40A	4	PCLKT4_0	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB8	PB22B	4	PCLKC4_0	C	PB40B	4	PCLKC4_0	C
AA9	PB23A	4	VREF2_4	T	PB41A	4	VREF2_4	T
Y9	PB23B	4	VREF1_4	C	PB41B	4	VREF1_4	C
AB9	PB24A	4	BDQS24	T	PB42A	4	BDQS42	T
GNDIO	GNDIO4	4			GNDIO4	4		
AB10	PB24B	4		C	PB42B	4		C
AA10	PB25A	4		T	PB43A	4		T
Y11	PB25B	4		C	PB43B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	4			GNDIO4	4		
V10	PB29A	4		T	PB47A	4		T
U11	PB29B	4		C	PB47B	4		C
V11	PB30A	4		T	PB48A	4		T
W11	PB30B	4		C	PB48B	4		C
AA11	PB31A	4		T	PB49A	4		T
AB11	PB31B	4		C	PB49B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
T11	PB32A	4		T	PB50A	4		T
U12	PB32B	4		C	PB50B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
AA12	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T
Y12	PB33B	4		C	PB51B	4		C
V12	PB34A	4		T	PB52A	4		T
W12	PB34B	4		C	PB52B	4		C
AB12	PB35A	4		T	PB53A	4		T
AA13	PB35B	4		C	PB53B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
T12	PB36A	4		T	PB54A	4		T
U13	PB36B	4		C	PB54B	4		C
V13	PB37A	4		T	PB55A	4		T
T13	PB37B	4		C	PB55B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
AB13	PB38A	4		T	PB56A	4		T
AB14	PB38B	4		C	PB56B	4		C
U14	PB39A	4		T	PB57A	4		T
T14	PB39B	4		C	PB57B	4		C
AA14	PB40A	4		T	PB58A	4		T
VCCIO	VCCIO4	4			VCCIO4	4		
Y14	PB40B	4		C	PB58B	4		C
W14	PB41A	4		T	PB59A	4		T
V14	PB41B	4		C	PB59B	4		C
AB15	PB42A	4	BDQS42	T	PB60A	4	BDQS60	T
GNDIO	GNDIO4	4			GNDIO4	4		

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
AA15	PB42B	4		C	PB60B	4		C
V15	PB43A	4		T	PB61A	4		T
U15	PB43B	4		C	PB61B	4		C
AB16	PB44A	4		T	PB62A	4		T
VCCIO	VCCIO4	4			VCCIO4	4		
AA16	PB44B	4		C	PB62B	4		C
AB17	PB45A	4		T	PB63A	4		T
AA17	PB45B	4		C	PB63B	4		C
Y15	PB46A	4		T	PB64A	4		T
GNDIO	GNDIO4	4			GNDIO4	4		
W15	PB46B	4		C	PB64B	4		C
AB20	PB47A	4		T	PB65A	4		T
AB21	PB47B	4		C	PB65B	4		C
AA21	PB48A	4		T	PB66A	4		T
AA20	PB48B	4		C	PB66B	4		C
AB19	PB49A	4		T	PB67A	4		T
AB18	PB49B	4		C	PB67B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
Y22	PB50A	4		T	PB68A	4		T
Y21	PB50B	4		C	PB68B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
Y17	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T
Y18	PB51B	4		C	PB69B	4		C
Y16	PB52A	4		T	PB70A	4		T
W17	PB52B	4		C	PB70B	4		C
Y19	PB53A	4		T	PB71A	4		T
Y20	PB53B	4		C	PB71B	4		C
VCCIO	VCCIO4	4			VCCIO4	4		
W19	PB54A	4		T	PB72A	4		T
W18	PB54B	4		C	PB72B	4		C
V17	PB55A	4		T	PB73A	4		T
V18	PB55B	4		C	PB73B	4		C
GNDIO	GNDIO4	4			GNDIO4	4		
W20	CFG2	8			CFG2	8		
V20	CFG1	8			CFG1	8		
V19	CFG0	8			CFG0	8		
V22	PROGRAMN	8			PROGRAMN	8		
W22	CCLK	8			CCLK	8		
U18	INITN	8			INITN	8		
U22	DONE	8			DONE	8		
GNDIO	GNDIO8	8			GNDIO8	8		
U20	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
U21	PR53A	8	CS1N	T	PR68A	8	CS1N	T
U17	PR52B	8	CSN	C	PR67B	8	CSN	C
U16	PR52A	8	D0	T	PR67A	8	D0	T
VCCIO	VCCIO8	8			VCCIO8	8		
T16	PR51B	8	D1	C	PR66B	8	D1	C
T17	PR51A	8	D2	T	PR66A	8	D2	T

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
T22	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	8			GNDIO8	8		
R22	PR50A	8	D4	T	PR65A	8	D4	T
T15	PR49B	8	D5	C	PR64B	8	D5	C
R17	PR49A	8	D6	T	PR64A	8	D6	T
T20	PR48B	8	D7	C	PR63B	8	D7	C
VCCIO	VCCIO8	8			VCCIO8	8		
T21	PR48A	8	DI	T	PR63A	8	DI	T
R21	PR47B	8	DOUT_CSON	C	PR62B	8	DOUT_CSON	C
R20	PR47A	8	BUSY	T	PR62A	8	BUSY	T
R16	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
R18	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	3			GNDIO3	3		
R19	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A	T
P22	PR44B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
P21	PR44A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
P16	PR43B	3	RLM0_GPLLC_IN_A**	C	PR58B	3	RLM0_GPLLC_IN_A**	C
VCCIO	VCCIO3	3			VCCIO3	3		
P17	PR43A	3	RLM0_GPLLT_IN_A**	T	PR58A	3	RLM0_GPLLT_IN_A**	T
P20	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A	C (LVDS)*
P19	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57	T (LVDS)*
GNDIO	GNDIO3	3			GNDIO3	3		
-	-	-			VCCIO3	3		
P18	PR41B	3		C	PR51B	3		C
N16	PR41A	3		T	PR51A	3		T
GNDIO	GNDIO3	3			GNDIO3	3		
N22	PR40B	3		C (LVDS)*	PR50B	3		C (LVDS)*
N21	PR40A	3		T (LVDS)*	PR50A	3		T (LVDS)*
N17	PR39B	3		C	PR49B	3		C
N18	PR39A	3		T	PR49A	3		T
VCCIO	VCCIO3	3			VCCIO3	3		
M22	PR38B	3		C (LVDS)*	PR48B	3		C (LVDS)*
M21	PR38A	3	RDQS38	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*
M16	PR37B	3		C	PR47B	3		C
GNDIO	GNDIO3	3			GNDIO3	3		
M17	PR37A	3		T	PR47A	3		T
M20	PR36B	3		C (LVDS)*	PR46B	3		C (LVDS)*
M19	PR36A	3		T (LVDS)*	PR46A	3		T (LVDS)*
M18	PR35B	3		C	PR45B	3		C
VCCIO	VCCIO3	3			VCCIO3	3		
L16	PR35A	3		T	PR45A	3		T
L22	PR34B	3		C (LVDS)*	PR44B	3		C (LVDS)*
L21	PR34A	3		T (LVDS)*	PR44A	3		T (LVDS)*
K22	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
K21	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
L17	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*
L18	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
GNDIO	GNDIO3	3			GNDIO3	3		
L20	PR30B	3		C	PR40B	3		C
L19	PR30A	3		T	PR40A	3		T
K16	PR29B	3		C (LVDS)*	PR39B	3		C (LVDS)*
K17	PR29A	3		T (LVDS)*	PR39A	3		T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
J16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
K18	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J22	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J21	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
H22	PR25B	2	PCLKC2_0	C	PR35B	2	PCLKC2_0	C
H21	PR25A	2	PCLKT2_0	T	PR35A	2	PCLKT2_0	T
GNDIO	GNDIO2	2			GNDIO2	2		
J17	PR24B	2		C (LVDS)*	PR34B	2		C (LVDS)*
J18	PR24A	2		T (LVDS)*	PR34A	2		T (LVDS)*
J20	PR23B	2		C	PR33B	2		C
J19	PR23A	2		T	PR33A	2		T
VCCIO	VCCIO2	2			VCCIO2	2		
H16	PR22B	2		C (LVDS)*	PR32B	2		C (LVDS)*
H17	PR22A	2	RDQS22	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
G22	PR21B	2		C	PR31B	2		C
GNDIO	GNDIO2	2			GNDIO2	2		
G21	PR21A	2		T	PR31A	2		T
H20	PR20B	2		C (LVDS)*	PR30B	2		C (LVDS)*
H19	PR20A	2		T (LVDS)*	PR30A	2		T (LVDS)*
G16	PR19B	2	RUM1_SPLLC_FB_A	C	PR29B	2	RUM1_SPLLC_FB_A	C
VCCIO	VCCIO2	2			VCCIO2	2		
H18	PR19A	2	RUM1_SPLLT_FB_A	T	PR29A	2	RUM1_SPLLT_FB_A	T
F22	PR18B	2	RUM1_SPLLC_IN_A	C (LVDS)*	PR28B	2	RUM1_SPLLC_IN_A	C (LVDS)*
F21	PR18A	2	RUM1_SPLLT_IN_A	T (LVDS)*	PR28A	2	RUM1_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO2	2			-	-		
G20	PR16B	2		C	PR26B	2		C
VCCIO	VCCIO2	2			-	-		
F20	PR16A	2		T	PR26A	2		T
-	-	-			GNDIO2	2		
G17	PR15B	2		C (LVDS)*	PR25B	2		C (LVDS)*
F17	PR15A	2		T (LVDS)*	PR25A	2		T (LVDS)*
-	-	-			VCCIO2	2		
GNDIO	GNDIO2	2			GNDIO2	2		
E22	PR14B	2		C	PR14B	2		C
D22	PR14A	2		T	PR14A	2		T
E20	PR13B	2		C (LVDS)*	PR13B	2		C (LVDS)*
D20	PR13A	2		T (LVDS)*	PR13A	2		T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
D19	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A	C
E19	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	2			GNDIO2	2		
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			-	-		
F16	XRES	-			XRES	-		
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
E13	PT28B	1		C	PT46B	1		C
D12	PT28A	1		T	PT46A	1		T
GNDIO	GNDIO1	1			GNDIO1	1		
A9	PT27B	1		C	PT45B	1		C
A8	PT27A	1		T	PT45A	1		T
A7	PT26B	1		C	PT44B	1		C
A6	PT26A	1		T	PT44A	1		T

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO1	1			VCCIO1	1		
E12	PT25B	1		C	PT43B	1		C
F12	PT25A	1		T	PT43A	1		T
A5	PT24B	1		C	PT42B	1		C
A4	PT24A	1		T	PT42A	1		T
GNDIO	GNDIO1	1			GNDIO1	1		
B7	PT23B	1		C	PT41B	1		C
B8	PT23A	1		T	PT41A	1		T
G11	PT22B	1		C	PT40B	1		C
E11	PT22A	1		T	PT40A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D11	PT21B	1	VREF2_1	C	PT39B	1	VREF2_1	C
D10	PT21A	1	VREF1_1	T	PT39A	1	VREF1_1	T
F11	PT20A	1	PCLKT1_0	T	PT38B	1	PCLKC1_0	C
G10	PT20B	1	PCLKC1_0	C	PT38A	1	PCLKT1_0	T
G9	PT19B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	0			GNDIO0	0		
F9	PT19A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
C9	PT18B	0	VREF2_0	C	PT36B	0	VREF2_0	C
D9	PT18A	0	VREF1_0	T	PT36A	0	VREF1_0	T
A2	PT17B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
A3	PT17A	0		T	PT35A	0		T
B3	PT16B	0		C	PT34B	0		C
C4	PT16A	0		T	PT34A	0		T
E10	PT15B	0		C	PT33B	0		C
F10	PT15A	0		T	PT33A	0		T
C7	PT14B	0		C	PT32B	0		C
GNDIO	GNDIO0	0			GNDIO0	0		
B6	PT14A	0		T	PT32A	0		T
C6	PT13B	0		C	PT31B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
C5	PT13A	0		T	PT31A	0		T
C8	PT12B	0		C	PT30B	0		C
D8	PT12A	0		T	PT30A	0		T
E8	PT11B	0		C	PT29B	0		C
E9	PT11A	0		T	PT29A	0		T
-	-	-			GNDIO0	0		
-	-	-			VCCIO0	0		
F8	PT10B	0		C	PT10B	0		C
G8	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	0			GNDIO0	0		
F7	PT9B	0		C	PT9B	0		C
G7	PT9A	0		T	PT9A	0		T
C3	PT8B	0		C	PT8B	0		C
D4	PT8A	0		T	PT8A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F6	PT7B	0		C	PT7B	0		C

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
E6	PT7A	0		T	PT7A	0		T
E5	PT6B	0		C	PT6B	0		C
D6	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	0			GNDIO0	0		
D3	PT5B	0		C	PT5B	0		C
E3	PT5A	0		T	PT5A	0		T
D5	PT4B	0		C	PT4B	0		C
E4	PT4A	0		T	PT4A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
C2	PT3B	0		C	PT3B	0		C
B2	PT3A	0		T	PT3A	0		T
B1	PT2B	0		C	PT2B	0		C
C1	PT2A	0		T	PT2A	0		T
R8	VCCPLL	-			VCCPLL	-		
H15	VCCPLL	-			VCCPLL	-		
H8	VCCPLL	-			VCCPLL	-		
R15	VCCPLL	-			VCCPLL	-		
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
B5	VCCIO0	0			VCCIO0	0		
B9	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
D13	VCCIO1	1			VCCIO1	1		
E16	VCCIO1	1			VCCIO1	1		
H14	VCCIO1	1			VCCIO1	1		
E21	VCCIO2	2			VCCIO2	2		
G18	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K19	VCCIO2	2			VCCIO2	2		
N19	VCCIO3	3			VCCIO3	3		
P15	VCCIO3	3			VCCIO3	3		
T18	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
AA18	VCCIO4	4			VCCIO4	4		
R14	VCCIO4	4			VCCIO4	4		
V16	VCCIO4	4			VCCIO4	4		
W13	VCCIO4	4			VCCIO4	4		
AA5	VCCIO5	5			VCCIO5	5		
R9	VCCIO5	5			VCCIO5	5		
V7	VCCIO5	5			VCCIO5	5		
W10	VCCIO5	5			VCCIO5	5		
N4	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
T5	VCCIO6	6			VCCIO6	6		
V2	VCCIO6	6			VCCIO6	6		
E2	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
J8	VCCIO7	7			VCCIO7	7		
K4	VCCIO7	7			VCCIO7	7		
AA22	VCCIO8	8			VCCIO8	8		
U19	VCCIO8	8			VCCIO8	8		
H11	VCCAUX	-			VCCAUX	-		
H12	VCCAUX	-			VCCAUX	-		
L15	VCCAUX	-			VCCAUX	-		
L8	VCCAUX	-			VCCAUX	-		
M15	VCCAUX	-			VCCAUX	-		
M8	VCCAUX	-			VCCAUX	-		
R11	VCCAUX	-			VCCAUX	-		
R12	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A16	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B13	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
D16	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
D7	GND	-			GND	-		
G19	GND	-			GND	-		
G4	GND	-			GND	-		
H10	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		

LFEM20E/20SE and LFE2M35E/35SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/20SE					LFE2M35E,/35SE			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
K11	GND	-			GND	-		
K12	GND	-			GND	-		
K13	GND	-			GND	-		
K15	GND	-			GND	-		
K20	GND	-			GND	-		
K3	GND	-			GND	-		
K8	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L12	GND	-			GND	-		
L13	GND	-			GND	-		
M10	GND	-			GND	-		
M11	GND	-			GND	-		
M12	GND	-			GND	-		
M13	GND	-			GND	-		
N10	GND	-			GND	-		
N11	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N15	GND	-			GND	-		
N20	GND	-			GND	-		
N3	GND	-			GND	-		
N8	GND	-			GND	-		
P14	GND	-			GND	-		
P9	GND	-			GND	-		
R10	GND	-			GND	-		
R13	GND	-			GND	-		
T19	GND	-			GND	-		
T4	GND	-			GND	-		
W16	GND	-			GND	-		
W2	GND	-			GND	-		
W21	GND	-			GND	-		
W7	GND	-			GND	-		
Y10	GND	-			GND	-		
Y13	GND	-			GND	-		
D15	NC	-			NC	-		
G14	NC	-			NC	-		
G15	NC	-			NC	-		
D14	NC	-			NC	-		
E15	NC	-			NC	-		
E14	NC	-			NC	-		
F15	NC	-			NC	-		
F14	NC	-			NC	-		
F13	NC	-			NC	-		
G12	NC	-			NC	-		
G13	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
C2	PL2A	7		T (LVDS)*
C1	PL2B	7		C (LVDS)*
F6	PL3A	7		T
H9	PL3B	7		C
D3	PL4A	7		T (LVDS)*
VCCIO	VCCIO7	7		
D2	PL4B	7		C (LVDS)*
F5	PL5A	7		T
H8	PL5B	7		C
E3	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	7		
E2	PL6B	7		C (LVDS)*
J9	PL7A	7		T
E4	PL7B	7		C
VCCIO	VCCIO7	7		
E1	PL8A	7		T (LVDS)*
D1	PL8B	7		C (LVDS)*
J8	PL9A	7	VREF2_7	T
F4	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	7		
F3	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
F1	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
G6	PL12A	7	LUM0_SPLLT_FB_A	T
K9	PL12B	7	LUM0_SPLLC_FB_A	C
G5	PL13A	7		T (LVDS)*
VCCIO	VCCIO7	7		
G4	PL13B	7		C (LVDS)*
H5	PL14A	7		T
H6	PL14B	7		C
GNDIO	GNDIO7	7		
J7	PL16A	7		T
H4	PL16B	7		C
VCCIO	VCCIO7	7		
H3	PL17A	7		T (LVDS)*
G3	PL17B	7		C (LVDS)*
GNDIO	GNDIO7	7		
G1	PL19A	7		T (LVDS)*
H1	PL19B	7		C (LVDS)*
J3	PL20A	7		T
J4	PL20B	7		C
VCCIO	VCCIO7	7		
H2	PL21A	7		T (LVDS)*

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
J2	PL21B	7		C (LVDS)*
K7	PL22A	7		T
J6	PL22B	7		C
GNDIO	GNDIO7	7		
K5	PL23A	7	LDQS23	T (LVDS)*
L5	PL23B	7		C (LVDS)*
K4	PL24A	7		T
VCCIO	VCCIO7	7		
L4	PL24B	7		C
K3	PL25A	7		T (LVDS)*
L3	PL25B	7		C (LVDS)*
J1	PL26A	7		T
GNDIO	GNDIO7	7		
K2	PL26B	7		C
K1	PL28A	7	LUM1_SPLLT_IN_A	T (LVDS)*
L1	PL28B	7	LUM1_SPLLC_IN_A	C (LVDS)*
K8	PL29A	7	LUM1_SPLLT_FB_A	T
M5	PL29B	7	LUM1_SPLLC_FB_A	C
VCCIO	VCCIO7	7		
M4	PL30A	7		T (LVDS)*
M3	PL30B	7		C (LVDS)*
L8	PL31A	7		T
M6	PL31B	7		C
GNDIO	GNDIO7	7		
M1	PL32A	7	LDQS32	T (LVDS)*
N1	PL32B	7		C (LVDS)*
N3	PL33A	7		T
VCCIO	VCCIO7	7		
N2	PL33B	7		C
N5	PL34A	7		T (LVDS)*
N4	PL34B	7		C (LVDS)*
M7	PL35A	7	PCLKT7_0	T
GNDIO	GNDIO7	7		
M8	PL35B	7	PCLKC7_0	C
P3	PL37A	6	PCLKT6_0	T (LVDS)*
P2	PL37B	6	PCLKC6_0	C (LVDS)*
P5	PL38A	6	VREF2_6	T
N6	PL38B	6	VREF1_6	C
P4	PL39A	6		T (LVDS)*
VCCIO	VCCIO6	6		
R3	PL39B	6		C (LVDS)*
P6	PL40A	6		T
P1	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
GNDIO	GNDIO6	6		
R1	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*
N8	PL42A	6	LLM2_SPLLT_FB_A	T
R5	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6		
T3	PL44A	6		T (LVDS)*
T4	PL44B	6		C (LVDS)*
P8	PL45A	6		T
R6	PL45B	6		C
VCCIO	VCCIO6	6		
T1	PL46A	6		T (LVDS)*
U1	PL46B	6		C (LVDS)*
R7	PL47A	6		T
T5	PL47B	6		C
GNDIO	GNDIO6	6		
U3	PL48A	6	LDQS48	T (LVDS)*
U4	PL48B	6		C (LVDS)*
U5	PL49A	6		T
VCCIO	VCCIO6	6		
U6	PL49B	6		C
U2	PL50A	6		T (LVDS)*
V1	PL50B	6		C (LVDS)*
W2	PL51A	6		T
GNDIO	GNDIO6	6		
V2	PL51B	6		C
V4	PL55A	6		T (LVDS)*
VCCIO	VCCIO6	6		
V3	PL55B	6		C (LVDS)*
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57	T (LVDS)*
GNDIO	GNDIO6	6		
W3	PL57B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
W1	PL58A	6	LLM0_GPLLT_FB_A	T
Y1	PL58B	6	LLM0_GPLLC_FB_A	C
VCCIO	VCCIO6	6		
AA1	PL59A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
AB1	PL59B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
U7	PL60A	6	LLM0_GDLLT_FB_A	T
V6	PL60B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	6		
T8	LLM0_PLLCAP	6		
W5	PL62A	6		T (LVDS)*
Y4	PL62B	6		C (LVDS)*
U8	PL63A	6		T

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
W6	PL63B	6		C
VCCIO	VCCIO6	6		
Y3	PL64A	6		T (LVDS)*
AA3	PL64B	6		C (LVDS)*
Y5	PL65B	6		C
GNDIO	GNDIO6	6		
AB2	PL66A	6	LDQS66	T (LVDS)*
AA4	PL66B	6		C (LVDS)*
Y6	PL67A	6		T
VCCIO	VCCIO6	6		
U9	PL67B	6		C
AA5	PL68A	6		T (LVDS)*
AA6	PL68B	6		C (LVDS)*
Y7	PL69A	6		T
GNDIO	GNDIO6	6		
V9	PL69B	6		C
AC3	TCK	-		
W8	TDI	-		
AC4	TMS	-		
V8	TDO	-		
AA7	VCCJ	-		
AB6	PB2A	5		T
Y8	PB2B	5		C
AD1	PB3A	5		T
AD2	PB3B	5		C
AC5	PB4A	5		T
VCCIO	VCCIO5	5		
AA8	PB4B	5		C
AC6	PB5A	5		T
W9	PB5B	5		C
AB7	PB6A	5	BDQS6	T
GNDIO	GNDIO5	5		
Y9	PB6B	5		C
AD3	PB7A	5		T
AD4	PB7B	5		C
AA9	PB8A	5		T
VCCIO	VCCIO5	5		
W10	PB8B	5		C
AC7	PB9A	5		T
Y10	PB9B	5		C
AE2	PB10A	5		T
GNDIO	GNDIO5	5		
AD5	PB10B	5		C

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
AE4	PB11A	5		T
AE3	PB11B	5		C
W11	PB12A	5		T
AB8	PB12B	5		C
AE5	PB13A	5		T
AD6	PB13B	5		C
VCCIO	VCCIO5	5		
AA10	PB14A	5		T
AC8	PB14B	5		C
GNDIO	GNDIO5	5		
W12	PB15A	5	BDQS15	T
AC9	PB15B	5		C
W13	PB16A	5		T
AB10	PB16B	5		C
AF3	PB17A	5		T
AF4	PB17B	5		C
VCCIO	VCCIO5	5		
AF5	PB18A	5		T
AF6	PB18B	5		C
Y12	PB19A	5		T
AB11	PB19B	5		C
GNDIO	GNDIO5	5		
AD7	PB20A	5		T
AF7	PB20B	5		C
AD8	PB21A	5		T
AA12	PB21B	5		C
AE8	PB22A	5		T
VCCIO	VCCIO5	5		
AF8	PB22B	5		C
AD9	PB23A	5		T
AC10	PB23B	5		C
AC11	PB24A	5	BDQS24	T
GNDIO	GNDIO5	5		
AB12	PB24B	5		C
AD10	PB25A	5		T
Y13	PB25B	5		C
AF9	PB26A	5		T
VCCIO	VCCIO5	5		
AE9	PB26B	5		C
AF10	PB27A	5		T
AE10	PB27B	5		C
AD11	PB28A	5		T
GNDIO	GNDIO5	5		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
AF11	PB28B	5		C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	5		
AA13	PB33A	5	BDQS33	T
AB13	PB33B	5		C
W14	PB34A	5	VREF2_5	T
AC12	PB34B	5	VREF1_5	C
AF12	PB35A	5	PCLKT5_0	T
AD12	PB35B	5	PCLKC5_0	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	5		
AC13	PB40A	4	PCLKT4_0	T
VCCIO	VCCIO4	4		
Y14	PB40B	4	PCLKC4_0	C
AE14	PB41A	4	VREF2_4	T
AC14	PB41B	4	VREF1_4	C
AB14	PB42A	4	BDQS42	T
GNDIO	GNDIO4	4		
AA14	PB42B	4		C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	4		
AF14	PB47A	4		T
AF15	PB47B	4		C
AC15	PB48A	4		T
AE15	PB48B	4		C
AB15	PB49A	4		T
AC16	PB49B	4		C
VCCIO	VCCIO4	4		
AE17	PB50A	4		T
AB16	PB50B	4		C
GNDIO	GNDIO4	4		
AA15	PB51A	4	BDQS51	T
AF17	PB51B	4		C
Y15	PB52A	4		T
AC17	PB52B	4		C
AF18	PB53A	4		T
AE18	PB53B	4		C
VCCIO	VCCIO4	4		
W15	PB54A	4		T
AB17	PB54B	4		C
AF20	PB55A	4		T
AE20	PB55B	4		C
GNDIO	GNDIO4	4		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
AB20	PB57A	4		T
AC19	PB57B	4		C
AC20	PB58A	4		T
VCCIO	VCCIO4	4		
AB19	PB59A	4		T
W16	PB59B	4		C
AA17	PB60A	4	BDQS60	T
GNDIO	GNDIO4	4		
AA18	PB61A	4		T
Y17	PB61B	4		C
AF21	PB62A	4		T
VCCIO	VCCIO4	4		
AC21	PB63A	4		T
AE21	PB63B	4		C
AF23	PB64A	4		T
GNDIO	GNDIO4	4		
W17	PB65A	4		T
AA19	PB65B	4		C
AE23	PB66B	4		C
AF24	PB67A	4		T
AE24	PB67B	4		C
VCCIO	VCCIO4	4		
Y18	PB68B	4		C
GNDIO	GNDIO4	4		
AC22	PB69A	4	BDQS69	T
AB21	PB69B	4		C
AD26	PB70B	4		C
AC23	PB71A	4		T
AC25	PB71B	4		C
VCCIO	VCCIO4	4		
W20	PB72B	4		C
V17	PB73A	4		T
AA20	PB73B	4		C
GNDIO	GNDIO4	4		
AA21	CFG2	8		
AA22	CFG1	8		
AB23	CFG0	8		
AC26	PROGRAMN	8		
AB24	CCLK	8		
AA23	INITN	8		
AB25	DONE	8		
GNDIO	GNDIO8	8		
Y19	PR68B	8	WRITEN	C

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
Y21	PR68A	8	CS1N	T
AB26	PR67B	8	CSN	C
Y22	PR67A	8	D0	T
VCCIO	VCCIO8	8		
W19	PR66B	8	D1	C
Y20	PR66A	8	D2	T
W22	PR65B	8	D3	C
GNDIO	GNDIO8	8		
W18	PR65A	8	D4	T
Y23	PR64B	8	D5	C
AA24	PR64A	8	D6	T
W21	PR63B	8	D7	C
VCCIO	VCCIO8	8		
V20	PR63A	8	DI	T
W23	PR62B	8	DOUT_CSON	C
Y24	PR62A	8	BUSY	T
V19	RLM0_PLLCAP	3		
V21	PR60B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	3		
U19	PR60A	3	RLM0_GDLLT_FB_A	T
AA26	PR59B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
Y26	PR59A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
V23	PR58B	3	RLM0_GPLLC_IN_A**	C
VCCIO	VCCIO3	3		
U20	PR58A	3	RLM0_GPLLT_IN_A**	T
W24	PR57B	3	RLM0_GPLLC_FB_A	C (LVDS)*
V24	PR57A	3	RLM0_GPLLT_FB_A/RDQS57	T (LVDS)*
GNDIO	GNDIO3	3		
U21	PR56A	3		T
W25	PR55B	3		C (LVDS)*
W26	PR55A	3		T (LVDS)*
VCCIO	VCCIO3	3		
U18	PR54B	3		C
U22	PR54A	3		T
V25	PR53B	3		C (LVDS)*
V26	PR53A	3		T (LVDS)*
U24	PR51B	3		C
T24	PR51A	3		T
GNDIO	GNDIO3	3		
T22	PR50B	3		C (LVDS)*
T23	PR50A	3		T (LVDS)*
U25	PR49B	3		C
U26	PR49A	3		T

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
VCCIO	VCCIO3	3		
T19	PR48B	3		C (LVDS)*
R19	PR48A	3	RDQS48	T (LVDS)*
R21	PR47B	3		C
GNDIO	GNDIO3	3		
R20	PR47A	3		T
T26	PR46B	3		C (LVDS)*
R26	PR46A	3		T (LVDS)*
P21	PR45B	3		C
VCCIO	VCCIO3	3		
P19	PR45A	3		T
R23	PR44B	3		C (LVDS)*
R24	PR44A	3		T (LVDS)*
R22	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3		
N19	PR42A	3	RLM2_SPLLT_FB_A	T
P23	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*
P24	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	3		
N21	PR40B	3		C
P22	PR40A	3		T
N20	PR39B	3		C (LVDS)*
N22	PR39A	3		T (LVDS)*
VCCIO	VCCIO3	3		
P25	PR38B	3	VREF2_3	C
P26	PR38A	3	VREF1_3	T
M21	PR37B	3	PCLKC3_0	C (LVDS)*
N23	PR37A	3	PCLKT3_0	T (LVDS)*
N24	PR35B	2	PCLKC2_0	C
N25	PR35A	2	PCLKT2_0	T
GNDIO	GNDIO2	2		
M22	PR34B	2		C (LVDS)*
M24	PR34A	2		T (LVDS)*
M23	PR33B	2		C
N26	PR33A	2		T
VCCIO	VCCIO2	2		
L22	PR32B	2		C (LVDS)*
L24	PR32A	2	RDQS32	T (LVDS)*
L23	PR31B	2		C
GNDIO	GNDIO2	2		
M20	PR31A	2		T
M26	PR30B	2		C (LVDS)*
L26	PR30A	2		T (LVDS)*

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
K22	PR29B	2	RUM1_SPLLC_FB_A	C
VCCIO	VCCIO2	2		
M19	PR29A	2	RUM1_SPLLT_FB_A	T
K25	PR28B	2	RUM1_SPLLC_IN_A	C (LVDS)*
K26	PR28A	2	RUM1_SPLLT_IN_A	T (LVDS)*
K24	PR26B	2		C
K23	PR26A	2		T
GNDIO	GNDIO2	2		
L19	PR25B	2		C (LVDS)*
K21	PR25A	2		T (LVDS)*
J23	PR24B	2		C
J24	PR24A	2		T
VCCIO	VCCIO2	2		
K20	PR23B	2		C (LVDS)*
J21	PR23A	2	RDQS23	T (LVDS)*
H21	PR22B	2		C
GNDIO	GNDIO2	2		
K18	PR22A	2		T
H22	PR21B	2		C (LVDS)*
J20	PR21A	2		T (LVDS)*
J25	PR20B	2		C
VCCIO	VCCIO2	2		
J26	PR20A	2		T
G21	PR19B	2		C (LVDS)*
J19	PR19A	2		T (LVDS)*
H23	PR18B	2		C
GNDIO	GNDIO2	2		
H24	PR18A	2		T
H25	PR17B	2		C (LVDS)*
H26	PR17A	2		T (LVDS)*
G22	PR16B	2		C
VCCIO	VCCIO2	2		
K19	PR16A	2		T
G24	PR15B	2		C (LVDS)*
G23	PR15A	2	RDQS15	T (LVDS)*
GNDIO	GNDIO2	2		
J18	PR14B	2		C
F22	PR14A	2		T
F23	PR13B	2		C (LVDS)*
F24	PR13A	2		T (LVDS)*
VCCIO	VCCIO2	2		
H20	PR12B	2	RUM0_SPLLC_FB_A	C
F21	PR12A	2	RUM0_SPLLT_FB_A	T

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
G26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*
F26	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*
E24	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	2		
E23	PR9A	2	VREF1_2	T
H19	XRES	-		
C25	URC_SQ_VCCRX0	12		
A24	URC_SQ_HDINP0	12		T
B25	URC_SQ_VCCIB0	12		
B24	URC_SQ_HDINN0	12		C
C22	URC_SQ_VCCTX0	12		
A21	URC_SQ_HDOUTP0	12		T
A22	URC_SQ_VCCOB0	12		
B21	URC_SQ_HDOUTN0	12		C
C21	URC_SQ_VCCTX1	12		
B20	URC_SQ_HDOUTN1	12		C
C20	URC_SQ_VCCOB1	12		
A20	URC_SQ_HDOUTP1	12		T
C24	URC_SQ_VCCRX1	12		
B23	URC_SQ_HDINN1	12		C
C23	URC_SQ_VCCIB1	12		
A23	URC_SQ_HDINP1	12		T
B19	URC_SQ_VCCAUX33	12		
E19	URC_SQ_REFCLKN	12		C
D19	URC_SQ_REFCLKP	12		T
C19	URC_SQ_VCCP	12		
A15	URC_SQ_HDINP2	12		T
C15	URC_SQ_VCCIB2	12		
B15	URC_SQ_HDINN2	12		C
C14	URC_SQ_VCCRX2	12		
A18	URC_SQ_HDOUTP2	12		T
C18	URC_SQ_VCCOB2	12		
B18	URC_SQ_HDOUTN2	12		C
C17	URC_SQ_VCCTX2	12		
B17	URC_SQ_HDOUTN3	12		C
A16	URC_SQ_VCCOB3	12		
A17	URC_SQ_HDOUTP3	12		T
C16	URC_SQ_VCCTX3	12		
B14	URC_SQ_HDINN3	12		C
B13	URC_SQ_VCCIB3	12		
A14	URC_SQ_HDINP3	12		T
C13	URC_SQ_VCCRX3	12		
E17	PT46B	1		C

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	Ball Function	Bank	Dual Function	Differential
D17	PT46A	1		T
GNDIO	GNDIO1	1		
F17	PT45B	1		C
D16	PT45A	1		T
F19	PT44B	1		C
F18	PT44A	1		T
VCCIO	VCCIO1	1		
E16	PT43B	1		C
D15	PT43A	1		T
G18	PT42B	1		C
E15	PT42A	1		T
GNDIO	GNDIO1	1		
G17	PT41B	1		C
E14	PT41A	1		T
D14	PT40B	1		C
D13	PT40A	1		T
VCCIO	VCCIO1	1		
F15	PT39B	1	VREF2_1	C
E12	PT39A	1	VREF1_1	T
H17	PT38B	1	PCLKC1_0	C
E13	PT38A	1	PCLKT1_0	T
C12	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	0		
G15	PT37A	0	PCLKT0_0	T
C11	PT36B	0	VREF2_0	C
F14	PT36A	0	VREF1_0	T
A12	PT35B	0		C
VCCIO	VCCIO0	0		
A11	PT35A	0		T
D12	PT34B	0		C
H16	PT34A	0		T
H18	PT33B	0		C
H15	PT33A	0		T
A10	PT32B	0		C
GNDIO	GNDIO0	0		
B10	PT32A	0		T
D11	PT31B	0		C
VCCIO	VCCIO0	0		
G14	PT31A	0		T
E11	PT30B	0		C
F13	PT30A	0		T
D10	PT29B	0		C
H14	PT29A	0		T

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
GNDIO	GNDIO0	0		
VCCIO	VCCIO0	0		
A9	PT24B	0		C
GNDIO	GNDIO0	0		
C10	PT23B	0		C
E8	PT23A	0		T
B9	PT22B	0		C
A8	PT22A	0		T
VCCIO	VCCIO0	0		
F12	PT21B	0		C
E10	PT21A	0		T
G13	PT20B	0		C
C9	PT20A	0		T
B8	PT19B	0		C
GNDIO	GNDIO0	0		
A7	PT19A	0		T
D9	PT18B	0		C
H13	PT18A	0		T
D6	PT17B	0		C
VCCIO	VCCIO0	0		
C7	PT17A	0		T
C8	PT16B	0		C
G12	PT16A	0		T
D8	PT15B	0		C
H12	PT15A	0		T
A6	PT14B	0		C
GNDIO	GNDIO0	0		
A5	PT14A	0		T
A4	PT13B	0		C
VCCIO	VCCIO0	0		
A3	PT13A	0		T
C6	PT12B	0		C
F10	PT12A	0		T
D7	PT11B	0		C
H11	PT11A	0		T
D5	PT10B	0		C
E6	PT10A	0		T
GNDIO	GNDIO0	0		
G10	PT9B	0		C
F9	PT9A	0		T
H10	PT8B	0		C
E7	PT8A	0		T
VCCIO	VCCIO0	0		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
B3	PT7B	0		C
C5	PT7A	0		T
B2	PT6B	0		C
C4	PT6A	0		T
GNDIO	GNDIO0	0		
G9	PT5B	0		C
F7	PT5A	0		T
C3	PT4B	0		C
D4	PT4A	0		T
VCCIO	VCCIO0	0		
J10	PT3B	0		C
F8	PT3A	0		T
G8	PT2B	0		C
G7	PT2A	0		T
H7	L_VCCPLL	-		
K6	L_VCCPLL	-		
P7	L_VCCPLL	-		
R8	L_VCCPLL	-		
V18	R_VCCPLL	-		
P20	R_VCCPLL	-		
J17	R_VCCPLL	-		
G19	R_VCCPLL	-		
AD13	VCC	-		
AD14	VCC	-		
AD16	VCC	-		
AD17	VCC	-		
AD19	VCC	-		
AD21	VCC	-		
AD22	VCC	-		
AD24	VCC	-		
AD25	VCC	-		
L12	VCC	-		
L13	VCC	-		
L14	VCC	-		
L15	VCC	-		
M11	VCC	-		
M12	VCC	-		
M15	VCC	-		
M16	VCC	-		
N11	VCC	-		
N16	VCC	-		
P11	VCC	-		
P16	VCC	-		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
R11	VCC	-		
R12	VCC	-		
R15	VCC	-		
R16	VCC	-		
T12	VCC	-		
T13	VCC	-		
T14	VCC	-		
T15	VCC	-		
B12	VCCIO0	0		
B7	VCCIO0	0		
F11	VCCIO0	0		
J13	VCCIO0	0		
K12	VCCIO0	0		
D18	VCCIO1	1		
F16	VCCIO1	1		
J14	VCCIO1	1		
K15	VCCIO1	1		
G25	VCCIO2	2		
L21	VCCIO2	2		
M17	VCCIO2	2		
M25	VCCIO2	2		
N18	VCCIO2	2		
P18	VCCIO3	3		
R17	VCCIO3	3		
R25	VCCIO3	3		
T21	VCCIO3	3		
Y25	VCCIO3	3		
AA16	VCCIO4	4		
AC18	VCCIO4	4		
U15	VCCIO4	4		
V14	VCCIO4	4		
AA11	VCCIO5	5		
AE12	VCCIO5	5		
AE7	VCCIO5	5		
U12	VCCIO5	5		
V13	VCCIO5	5		
P9	VCCIO6	6		
R10	VCCIO6	6		
R2	VCCIO6	6		
T6	VCCIO6	6		
Y2	VCCIO6	6		
G2	VCCIO7	7		
L6	VCCIO7	7		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
M10	VCCIO7	7		
M2	VCCIO7	7		
N9	VCCIO7	7		
AC24	VCCIO8	8		
U17	VCCIO8	8		
AE19	VCCAUX	-		
J11	VCCAUX	-		
J12	VCCAUX	-		
J15	VCCAUX	-		
J16	VCCAUX	-		
L18	VCCAUX	-		
L9	VCCAUX	-		
M18	VCCAUX	-		
M9	VCCAUX	-		
R18	VCCAUX	-		
R9	VCCAUX	-		
T18	VCCAUX	-		
T9	VCCAUX	-		
V11	VCCAUX	-		
V12	VCCAUX	-		
V15	VCCAUX	-		
V16	VCCAUX	-		
A13	GND	-		
A19	GND	-		
A2	GND	-		
A25	GND	-		
AA2	GND	-		
AA25	GND	-		
AB18	GND	-		
AB22	GND	-		
AB5	GND	-		
AB9	GND	-		
AE1	GND	-		
AE11	GND	-		
AE16	GND	-		
AE22	GND	-		
AE26	GND	-		
AE6	GND	-		
AF13	GND	-		
AF19	GND	-		
AF2	GND	-		
AF25	GND	-		
B1	GND	-		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
B11	GND	-		
B16	GND	-		
B22	GND	-		
B26	GND	-		
B6	GND	-		
E18	GND	-		
E22	GND	-		
E5	GND	-		
E9	GND	-		
F2	GND	-		
F25	GND	-		
G11	GND	-		
G16	GND	-		
J22	GND	-		
J5	GND	-		
K11	GND	-		
K13	GND	-		
K14	GND	-		
K16	GND	-		
L10	GND	-		
L11	GND	-		
L16	GND	-		
L17	GND	-		
L2	GND	-		
L20	GND	-		
L25	GND	-		
L7	GND	-		
M13	GND	-		
M14	GND	-		
N10	GND	-		
N12	GND	-		
N13	GND	-		
N14	GND	-		
N15	GND	-		
N17	GND	-		
P10	GND	-		
P12	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P17	GND	-		
R13	GND	-		
R14	GND	-		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
T10	GND	-		
T11	GND	-		
T16	GND	-		
T17	GND	-		
T2	GND	-		
T20	GND	-		
T25	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		
U16	GND	-		
V22	GND	-		
V5	GND	-		
Y11	GND	-		
Y16	GND	-		
AB3	NC	-		
AB4	NC	-		
AC1	NC	-		
AC2	NC	-		
AD15	NC	-		
AD18	NC	-		
AD20	NC	-		
AD23	NC	-		
AE13	NC	-		
AE25	NC	-		
AF16	NC	-		
AF22	NC	-		
B4	NC	-		
B5	NC	-		
C26	NC	-		
D20	NC	-		
D21	NC	-		
D22	NC	-		
D23	NC	-		
D24	NC	-		
D25	NC	-		
D26	NC	-		
E20	NC	-		
E21	NC	-		
E25	NC	-		
E26	NC	-		
F20	NC	-		

LFE2M35E/35SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/35SE				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
G20	NC	-		
K10	NC	-		
K17	NC	-		
R4	NC	-		
U10	NC	-		
U23	NC	-		
V10	NC	-		
W7	NC	-		
N7	NC	-		
V7	NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

LatticeECP2/M Family Data Sheet Ordering Information

April 2007 Advance Data Sheet DS1006

LatticeECP2 Part Number Description

LFE2 – XX XE – X XXXXXX X

Device Family
ECP2 (LatticeECP2 FPGA)

Logic Capacity
6 = 6K LUTs
12 = 12K LUTs
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs

Encryption
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

Supply Voltage
E = 1.2V

Grade
C = Commercial
I = Industrial

Package
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FN256 = 256-ball Lead-Free fpBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN900 = 900-ball Lead-Free fpBGA

Speed
5 = Slowest
6
7 = Fastest

Ordering Information

Note: LatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Contact Your Local Lattice Sales Representative for Product Availability.

LatticeECP2 Standard Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144C	90	1.2V	-5	TQFP	144	COM	6
LFE2-6E-6T144C	90	1.2V	-6	TQFP	144	COM	6
LFE2-6E-7T144C	90	1.2V	-7	TQFP	144	COM	6
LFE2-6E-5F256C	190	1.2V	-5	fpBGA	256	COM	6
LFE2-6E-6F256C	190	1.2V	-6	fpBGA	256	COM	6
LFE2-6E-7F256C	190	1.2V	-7	fpBGA	256	COM	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144C	93	1.2V	-5	TQFP	144	COM	12
LFE2-12E-6T144C	93	1.2V	-6	TQFP	144	COM	12
LFE2-12E-7T144C	93	1.2V	-7	TQFP	144	COM	12
LFE2-12E-5Q208C	131	1.2V	-5	PQFP	208	COM	12
LFE2-12E-6Q208C	131	1.2V	-6	PQFP	208	COM	12
LFE2-12E-7Q208C	131	1.2V	-7	PQFP	208	COM	12
LFE2-12E-5F256C	193	1.2V	-5	fpBGA	256	COM	12
LFE2-12E-6F256C	193	1.2V	-6	fpBGA	256	COM	12
LFE2-12E-7F256C	193	1.2V	-7	fpBGA	256	COM	12
LFE2-12E-5F484C	297	1.2V	-5	fpBGA	484	COM	12
LFE2-12E-6F484C	297	1.2V	-6	fpBGA	484	COM	12
LFE2-12E-7F484C	297	1.2V	-7	fpBGA	484	COM	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5Q208C	131	1.2V	-5	PQFP	208	COM	20
LFE2-20E-6Q208C	131	1.2V	-6	PQFP	208	COM	20
LFE2-20E-7Q208C	131	1.2V	-7	PQFP	208	COM	20
LFE2-20E-5F256C	193	1.2V	-5	fpBGA	256	COM	20
LFE2-20E-6F256C	193	1.2V	-6	fpBGA	256	COM	20
LFE2-20E-7F256C	193	1.2V	-7	fpBGA	256	COM	20
LFE2-20E-5F484C	331	1.2V	-5	fpBGA	484	COM	20
LFE2-20E-6F484C	331	1.2V	-6	fpBGA	484	COM	20
LFE2-20E-7F484C	331	1.2V	-7	fpBGA	484	COM	20
LFE2-20E-5F672C	402	1.2V	-5	fpBGA	672	COM	20
LFE2-20E-6F672C	402	1.2V	-6	fpBGA	672	COM	20
LFE2-20E-7F672C	402	1.2V	-7	fpBGA	672	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484C	331	1.2V	-5	fpBGA	484	COM	35
LFE2-35E-6F484C	331	1.2V	-6	fpBGA	484	COM	35
LFE2-35E-7F484C	331	1.2V	-7	fpBGA	484	COM	35
LFE2-35E-5F672C	450	1.2V	-5	fpBGA	672	COM	35
LFE2-35E-6F672C	450	1.2V	-6	fpBGA	672	COM	35
LFE2-35E-7F672C	450	1.2V	-7	fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484C	339	1.2V	-5	fpBGA	484	COM	50
LFE2-50E-6F484C	339	1.2V	-6	fpBGA	484	COM	50
LFE2-50E-7F484C	339	1.2V	-7	fpBGA	484	COM	50
LFE2-50E-5F672C	500	1.2V	-5	fpBGA	672	COM	50
LFE2-50E-6F672C	500	1.2V	-6	fpBGA	672	COM	50
LFE2-50E-7F672C	500	1.2V	-7	fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672C	500	1.2V	-5	fpBGA	672	COM	70
LFE2-70E-6F672C	500	1.2V	-6	fpBGA	672	COM	70
LFE2-70E-7F672C	500	1.2V	-7	fpBGA	672	COM	70
LFE2-70E-5F900C	588	1.2V	-5	fpBGA	900	COM	70
LFE2-70E-6F900C	588	1.2V	-6	fpBGA	900	COM	70
LFE2-70E-7F900C	588	1.2V	-7	fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144I	90	1.2V	-5	TQFP	144	IND	6
LFE2-6E-6T144I	90	1.2V	-6	TQFP	144	IND	6
LFE2-6E-5F256I	190	1.2V	-5	fpBGA	256	IND	6
LFE2-6E-6F256I	190	1.2V	-6	fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144I	93	1.2V	-5	TQFP	144	IND	12
LFE2-12E-6T144I	93	1.2V	-6	TQFP	144	IND	12
LFE2-12E-5Q208I	131	1.2V	-5	PQFP	208	IND	12
LFE2-12E-6Q208I	131	1.2V	-6	PQFP	208	IND	12
LFE2-12E-5F256I	193	1.2V	-5	fpBGA	256	IND	12
LFE2-12E-6F256I	193	1.2V	-6	fpBGA	256	IND	12
LFE2-12E-5F484I	297	1.2V	-5	fpBGA	484	IND	12
LFE2-12E-6F484I	297	1.2V	-6	fpBGA	484	IND	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5Q208I	131	1.2V	-5	PQFP	208	IND	20
LFE2-20E-6Q208I	131	1.2V	-6	PQFP	208	IND	20
LFE2-20E-5F256I	193	1.2V	-5	fpBGA	256	IND	20
LFE2-20E-6F256I	193	1.2V	-6	fpBGA	256	IND	20
LFE2-20E-5F484I	331	1.2V	-5	fpBGA	484	IND	20
LFE2-20E-6F484I	331	1.2V	-6	fpBGA	484	IND	20
LFE2-20E-5F672I	402	1.2V	-5	fpBGA	672	IND	20
LFE2-20E-6F672I	402	1.2V	-6	fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484I	331	1.2V	-5	fpBGA	484	IND	35
LFE2-35E-6F484I	331	1.2V	-6	fpBGA	484	IND	35
LFE2-35E-5F672I	450	1.2V	-5	fpBGA	672	IND	35
LFE2-35E-6F672I	450	1.2V	-6	fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484I	339	1.2V	-5	fpBGA	484	IND	50
LFE2-50E-6F484I	339	1.2V	-6	fpBGA	484	IND	50
LFE2-50E-5F672I	500	1.2V	-5	fpBGA	672	IND	50
LFE2-50E-6F672I	500	1.2V	-6	fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672I	500	1.2V	-5	fpBGA	672	IND	70
LFE2-70E-6F672I	500	1.2V	-6	fpBGA	672	IND	70
LFE2-70E-5F900I	588	1.2V	-5	fpBGA	900	IND	70
LFE2-70E-6F900I	588	1.2V	-6	fpBGA	900	IND	70

LatticeECP2 Standard Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	COM	6
LFE2-6E-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	COM	6
LFE2-6E-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	COM	6
LFE2-6E-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	COM	6
LFE2-6E-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	COM	6
LFE2-6E-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	COM	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	COM	12
LFE2-12E-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	COM	12
LFE2-12E-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	COM	12
LFE2-12E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	12
LFE2-12E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	12
LFE2-12E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	12
LFE2-12E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	12
LFE2-12E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	12
LFE2-12E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	12
LFE2-12E-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	COM	12
LFE2-12E-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	COM	12
LFE2-12E-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	COM	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	20
LFE2-20E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	20
LFE2-20E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	20
LFE2-20E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2-20E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2-20E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	20
LFE2-20E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2-20E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2-20E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2-20E-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	COM	20
LFE2-20E-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	COM	20
LFE2-20E-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2-35E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2-35E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2-35E-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2-35E-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2-35E-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2-50E-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2-50E-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	COM	50
LFE2-50E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2-50E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2-50E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	70
LFE2-70E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	70
LFE2-70E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	70
LFE2-70E-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2-70E-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2-70E-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	IND	6
LFE2-6E-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	IND	6
LFE2-6E-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	IND	6
LFE2-6E-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	IND	12
LFE2-12E-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	IND	12
LFE2-12E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	12
LFE2-12E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	12
LFE2-12E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	12
LFE2-12E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	12
LFE2-12E-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	IND	12
LFE2-12E-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	IND	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	20
LFE2-20E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	20
LFE2-20E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2-20E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	20
LFE2-20E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2-20E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2-20E-5FN672I	402	1.2V	-5	Lead-Free fpBGA	672	IND	20
LFE2-20E-6FN672I	402	1.2V	-6	Lead-Free fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2-35E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2-35E-5FN672I	450	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2-35E-6FN672I	450	1.2V	-6	Lead-Free fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484I	339	1.2V	-5	Lead-Free fpBGA	484	IND	50
LFE2-50E-6FN484I	339	1.2V	-6	Lead-Free fpBGA	484	IND	50
LFE2-50E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	50
LFE2-50E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	70
LFE2-70E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	70
LFE2-70E-5FN900I	583	1.2V	-5	Lead-Free fpBGA	900	IND	70
LFE2-70E-6FN900I	583	1.2V	-6	Lead-Free fpBGA	900	IND	70

LatticeECP2 S-Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144C	90	1.2V	-5	TQFP	144	Com	6
LFE2-6SE-6T144C	90	1.2V	-6	TQFP	144	Com	6
LFE2-6SE-7T144C	90	1.2V	-7	TQFP	144	Com	6
LFE2-6SE-5F256C	190	1.2V	-5	fpBGA	256	Com	6
LFE2-6SE-6F256C	190	1.2V	-6	fpBGA	256	Com	6
LFE2-6SE-7F256C	190	1.2V	-7	fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144C	93	1.2V	-5	TQFP	144	Com	12
LFE2-12SE-6T144C	93	1.2V	-6	TQFP	144	Com	12
LFE2-12SE-7T144C	93	1.2V	-7	TQFP	144	Com	12
LFE2-12SE-5Q208C	131	1.2V	-5	PQFP	208	Com	12
LFE2-12SE-6Q208C	131	1.2V	-6	PQFP	208	Com	12
LFE2-12SE-7Q208C	131	1.2V	-7	PQFP	208	Com	12
LFE2-12SE-5F256C	193	1.2V	-5	fpBGA	256	Com	12
LFE2-12SE-6F256C	193	1.2V	-6	fpBGA	256	Com	12
LFE2-12SE-7F256C	193	1.2V	-7	fpBGA	256	Com	12
LFE2-12SE-5F484C	297	1.2V	-5	fpBGA	484	Com	12
LFE2-12SE-6F484C	297	1.2V	-6	fpBGA	484	Com	12
LFE2-12SE-7F484C	297	1.2V	-7	fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5Q208C	131	1.2V	-5	PQFP	208	Com	20
LFE2-20SE-6Q208C	131	1.2V	-6	PQFP	208	Com	20
LFE2-20SE-7Q208C	131	1.2V	-7	PQFP	208	Com	20
LFE2-20SE-5F256C	193	1.2V	-5	fpBGA	256	Com	20
LFE2-20SE-6F256C	193	1.2V	-6	fpBGA	256	Com	20
LFE2-20SE-7F256C	193	1.2V	-7	fpBGA	256	Com	20
LFE2-20SE-5F484C	331	1.2V	-5	fpBGA	484	Com	20
LFE2-20SE-6F484C	331	1.2V	-6	fpBGA	484	Com	20
LFE2-20SE-7F484C	331	1.2V	-7	fpBGA	484	Com	20
LFE2-20SE-5F672C	402	1.2V	-5	fpBGA	672	Com	20
LFE2-20SE-6F672C	402	1.2V	-6	fpBGA	672	Com	20
LFE2-20SE-7F672C	402	1.2V	-7	fpBGA	672	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	588	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	588	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	588	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	20
LFE2-20SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	20
LFE2-20SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	20
LFE2-20SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	20
LFE2-20SE-5F484I	331	1.2V	-5	fpBGA	484	Ind	20
LFE2-20SE-6F484I	331	1.2V	-6	fpBGA	484	Ind	20
LFE2-20SE-5F672I	402	1.2V	-5	fpBGA	672	Ind	20
LFE2-20SE-6F672I	402	1.2V	-6	fpBGA	672	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484I	331	1.2V	-5	fpBGA	484	Ind	35
LFE2-35SE-6F484I	331	1.2V	-6	fpBGA	484	Ind	35
LFE2-35SE-5F672I	450	1.2V	-5	fpBGA	672	Ind	35
LFE2-35SE-6F672I	450	1.2V	-6	fpBGA	672	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484I	339	1.2V	-5	fpBGA	484	Ind	50
LFE2-50SE-6F484I	339	1.2V	-6	fpBGA	484	Ind	50
LFE2-50SE-5F672I	500	1.2V	-5	fpBGA	672	Ind	50
LFE2-50SE-6F672I	500	1.2V	-6	fpBGA	672	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672I	500	1.2V	-5	fpBGA	672	Ind	70
LFE2-70SE-6F672I	500	1.2V	-6	fpBGA	672	Ind	70
LFE2-70SE-5F900I	588	1.2V	-5	fpBGA	900	Ind	70
LFE2-70SE-6F900I	588	1.2V	-6	fpBGA	900	Ind	70

LatticeECP2 S-Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	Com	6
LFE2-6SE-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	Com	6
LFE2-6SE-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	Com	6
LFE2-6SE-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	Com	6
LFE2-6SE-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	Com	6
LFE2-6SE-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	Com	12
LFE2-12SE-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	Com	12
LFE2-12SE-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	Com	12
LFE2-12SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	12
LFE2-12SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	12
LFE2-12SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	12
LFE2-12SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	12
LFE2-12SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	12
LFE2-12SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	12
LFE2-12SE-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	Com	12
LFE2-12SE-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	Com	12
LFE2-12SE-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	20
LFE2-20SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	20
LFE2-20SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	20
LFE2-20SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2-20SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2-20SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	20
LFE2-20SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2-20SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2-20SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2-20SE-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	Com	20
LFE2-20SE-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	Com	20
LFE2-20SE-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2-35SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2-35SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2-35SE-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2-35SE-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2-35SE-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2-50SE-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2-50SE-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	Com	50
LFE2-50SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2-50SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2-50SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	70
LFE2-70SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	70
LFE2-70SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	70
LFE2-70SE-5FN900C	588	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2-70SE-6FN900C	588	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2-70SE-7FN900C	588	1.2V	-7	Lead-Free fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	Ind	6
LFE2-6SE-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	Ind	6
LFE2-6SE-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	Ind	6
LFE2-6SE-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	Ind	12
LFE2-12SE-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	Ind	12
LFE2-12SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	12
LFE2-12SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	12
LFE2-12SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	Ind	12
LFE2-12SE-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	Ind	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	20
LFE2-20SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	20
LFE2-20SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2-20SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	20
LFE2-20SE-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2-20SE-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2-20SE-5FN672I	402	1.2V	-5	Lead-Free fpBGA	672	Ind	20
LFE2-20SE-6FN672I	402	1.2V	-6	Lead-Free fpBGA	672	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2-35SE-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2-35SE-5FN672I	450	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2-35SE-6FN672I	450	1.2V	-6	Lead-Free fpBGA	672	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484I	339	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2-50SE-6FN484I	339	1.2V	-6	Lead-Free fpBGA	484	Ind	50
LFE2-50SE-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2-50SE-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	Ind	70
LFE2-70SE-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	Ind	70
LFE2-70SE-5FN900I	588	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2-70SE-6FN900I	588	1.2V	-6	Lead-Free fpBGA	900	Ind	70

LatticeECP2M Part Number Description

LFE2M XXX XE – X XXXXXX X

Device Family
ECP2M (LatticeECP2 FPGA + SERDES)

Logic Capacity
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs
100 = 100K LUTs

Encryption
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

Supply Voltage
E = 1.2V

Grade
C = Commercial
I = Industrial

Package
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
F1152 = 1152-ball fpBGA
F1156 = 1156-ball fpBGA
FN256 = 256-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA
FN672 = 672-ball Lead-free fpBGA
FN900 = 900-ball Lead-free fpBGA
FN1152 = 1152-ball Lead-free fpBGA
FN1156 = 1156-ball Lead-free fpBGA

Speed
5 = Slowest
6
7 = Fastest

Ordering Information

Note: LatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:

Contact Your Local Lattice Sales Representative for Product Availability.

LatticeECP2M Standard Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484C	304	1.2V	-5	fpBGA	484	COM	20
LFE2M20E-6F484C	304	1.2V	-6	fpBGA	484	COM	20
LFE2M20E-7F484C	304	1.2V	-7	fpBGA	484	COM	20
LFE2M20E-5F256C	140	1.2V	-5	fpBGA	256	COM	20
LFE2M20E-6F256C	140	1.2V	-6	fpBGA	256	COM	20
LFE2M20E-7F256C	140	1.2V	-7	fpBGA	256	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672C	410	1.2V	-5	fpBGA	672	COM	35
LFE2M35E-6F672C	410	1.2V	-6	fpBGA	672	COM	35
LFE2M35E-7F672C	410	1.2V	-7	fpBGA	672	COM	35
LFE2M35E-5F484C	303	1.2V	-5	fpBGA	484	COM	35
LFE2M35E-6F484C	303	1.2V	-6	fpBGA	484	COM	35
LFE2M35E-7F484C	303	1.2V	-7	fpBGA	484	COM	35
LFE2M35E-5F256C	140	1.2V	-5	fpBGA	256	COM	35
LFE2M35E-6F256C	140	1.2V	-6	fpBGA	256	COM	35
LFE2M35E-7F256C	140	1.2V	-7	fpBGA	256	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900C	410	1.2V	-5	fpBGA	900	COM	50
LFE2M50E-6F900C	410	1.2V	-6	fpBGA	900	COM	50
LFE2M50E-7F900C	410	1.2V	-7	fpBGA	900	COM	50
LFE2M50E-5F672C	372	1.2V	-5	fpBGA	672	COM	50
LFE2M50E-6F672C	372	1.2V	-6	fpBGA	672	COM	50
LFE2M50E-7F672C	372	1.2V	-7	fpBGA	672	COM	50
LFE2M50E-5F484C	270	1.2V	-5	fpBGA	484	COM	50
LFE2M50E-6F484C	270	1.2V	-6	fpBGA	484	COM	50
LFE2M50E-7F484C	270	1.2V	-7	fpBGA	484	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152C	430	1.2V	-5	fpBGA	1152	COM	70
LFE2M70E-6F1152C	430	1.2V	-6	fpBGA	1152	COM	70
LFE2M70E-7F1152C	430	1.2V	-7	fpBGA	1152	COM	70
LFE2M70E-5F900C	416	1.2V	-5	fpBGA	900	COM	70
LFE2M70E-6F900C	416	1.2V	-6	fpBGA	900	COM	70
LFE2M70E-7F900C	416	1.2V	-7	fpBGA	900	COM	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1156C	616	1.2V	-5	fpBGA	1156	COM	100
LFE2M100E-6F1156C	616	1.2V	-6	fpBGA	1156	COM	100
LFE2M100E-7F1156C	616	1.2V	-7	fpBGA	1156	COM	100
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484I	304	1.2V	-5	fpBGA	484	IND	20
LFE2M20E-6F484I	304	1.2V	-6	fpBGA	484	IND	20
LFE2M20E-5F256I	140	1.2V	-5	fpBGA	256	IND	20
LFE2M20E-6F256I	140	1.2V	-6	fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672I	410	1.2V	-5	fpBGA	672	IND	35
LFE2M35E-6F672I	410	1.2V	-6	fpBGA	672	IND	35
LFE2M35E-5F484I	303	1.2V	-5	fpBGA	484	IND	35
LFE2M35E-6F484I	303	1.2V	-6	fpBGA	484	IND	35
LFE2M35E-5F256I	140	1.2V	-5	fpBGA	256	IND	35
LFE2M35E-6F256I	140	1.2V	-6	fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900I	410	1.2V	-5	fpBGA	900	IND	50
LFE2M50E-6F900I	410	1.2V	-6	fpBGA	900	IND	50
LFE2M50E-5F672I	372	1.2V	-5	fpBGA	672	IND	50
LFE2M50E-6F672I	372	1.2V	-6	fpBGA	672	IND	50
LFE2M50E-5F484I	270	1.2V	-5	fpBGA	484	IND	50
LFE2M50E-6F484I	270	1.2V	-6	fpBGA	484	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152I	430	1.2V	-5	fpBGA	1152	IND	70
LFE2M70E-6F1152I	430	1.2V	-6	fpBGA	1152	IND	70
LFE2M70E-5F900I	416	1.2V	-5	fpBGA	900	IND	70
LFE2M70E-6F900I	416	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1156I	616	1.2V	-5	fpBGA	1156	IND	100
LFE2M100E-6F1156I	616	1.2V	-6	fpBGA	1156	IND	100
LFE2M100E-5F1152I	520	1.2V	-5	fpBGA	1152	IND	100
LFE2M100E-6F1152I	520	1.2V	-6	fpBGA	1152	IND	100
LFE2M100E-5F900I	416	1.2V	-5	fpBGA	900	IND	100
LFE2M100E-6F900I	416	1.2V	-6	fpBGA	900	IND	100

LatticeECP2M Standard Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2M20E-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2M20E-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2M20E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2M20E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2M20E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2M35E-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2M35E-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	COM	35
LFE2M35E-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2M35E-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2M35E-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2M35E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	35
LFE2M35E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	35
LFE2M35E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	COM	50
LFE2M50E-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	COM	50
LFE2M50E-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	COM	50
LFE2M50E-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2M50E-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2M50E-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	COM	50
LFE2M50E-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2M50E-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2M50E-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152C	430	1.2V	-5	Lead-Free fpBGA	1152	COM	70
LFE2M70E-6FN1152C	430	1.2V	-6	Lead-Free fpBGA	1152	COM	70
LFE2M70E-7FN1152C	430	1.2V	-7	Lead-Free fpBGA	1152	COM	70
LFE2M70E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2M70E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2M70E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1156C	616	1.2V	-5	Lead-Free fpBGA	1156	COM	100
LFE2M100E-6FN1156C	616	1.2V	-6	Lead-Free fpBGA	1156	COM	100
LFE2M100E-7FN1156C	616	1.2V	-7	Lead-Free fpBGA	1156	COM	100
LFE2M100E-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	COM	100
LFE2M100E-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	COM	100
LFE2M100E-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	COM	100
LFE2M100E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	100
LFE2M100E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	100
LFE2M100E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2M20E-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2M20E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2M20E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2M35E-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	IND	35
LFE2M35E-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2M35E-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2M35E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	35
LFE2M35E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50E-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50E-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50E-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50E-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50E-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152I	430	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-6FN1152I	430	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1156I	616	1.2V	-5	Lead-Free fpBGA	1156	Ind	100
LFE2M100E-6FN1156I	616	1.2V	-6	Lead-Free fpBGA	1156	Ind	100
LFE2M100E-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484C	304	1.2V	-5	fpBGA	484	Com	20
LFE2M20SE-6F484C	304	1.2V	-6	fpBGA	484	Com	20
LFE2M20SE-7F484C	304	1.2V	-7	fpBGA	484	Com	20
LFE2M20SE-5F256C	140	1.2V	-5	fpBGA	256	Com	20
LFE2M20SE-6F256C	140	1.2V	-6	fpBGA	256	Com	20
LFE2M20SE-7F256C	140	1.2V	-7	fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672C	410	1.2V	-5	fpBGA	672	Com	35
LFE2M35SE-6F672C	410	1.2V	-6	fpBGA	672	Com	35
LFE2M35SE-7F672C	410	1.2V	-7	fpBGA	672	Com	35
LFE2M35SE-5F484C	303	1.2V	-5	fpBGA	484	Com	35
LFE2M35SE-6F484C	303	1.2V	-6	fpBGA	484	Com	35
LFE2M35SE-7F484C	303	1.2V	-7	fpBGA	484	Com	35
LFE2M35SE-5F256C	140	1.2V	-5	fpBGA	256	Com	35
LFE2M35SE-6F256C	140	1.2V	-6	fpBGA	256	Com	35
LFE2M35SE-7F256C	140	1.2V	-7	fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900C	410	1.2V	-5	fpBGA	900	Com	50
LFE2M50SE-6F900C	410	1.2V	-6	fpBGA	900	Com	50
LFE2M50SE-7F900C	410	1.2V	-7	fpBGA	900	Com	50
LFE2M50SE-5F672C	372	1.2V	-5	fpBGA	672	Com	50
LFE2M50SE-6F672C	372	1.2V	-6	fpBGA	672	Com	50
LFE2M50SE-7F672C	372	1.2V	-7	fpBGA	672	Com	50
LFE2M50SE-5F484C	270	1.2V	-5	fpBGA	484	Com	50
LFE2M50SE-6F484C	270	1.2V	-6	fpBGA	484	Com	50
LFE2M50SE-7F484C	270	1.2V	-7	fpBGA	484	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152C	430	1.2V	-5	fpBGA	1152	Com	70
LFE2M70SE-6F1152C	430	1.2V	-6	fpBGA	1152	Com	70
LFE2M70SE-7F1152C	430	1.2V	-7	fpBGA	1152	Com	70
LFE2M70SE-5F900C	416	1.2V	-5	fpBGA	900	Com	70
LFE2M70SE-6F900C	416	1.2V	-6	fpBGA	900	Com	70
LFE2M70SE-7F900C	416	1.2V	-7	fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1156C	616	1.2V	-5	fpBGA	1156	Com	100
LFE2M100SE-6F1156C	616	1.2V	-6	fpBGA	1156	Com	100
LFE2M100SE-7F1156C	616	1.2V	-7	fpBGA	1156	Com	100
LFE2M100SE-5F1152C	520	1.2V	-5	fpBGA	1152	Com	100
LFE2M100SE-6F1152C	520	1.2V	-6	fpBGA	1152	Com	100
LFE2M100SE-7F1152C	520	1.2V	-7	fpBGA	1152	Com	100
LFE2M100SE-5F900C	416	1.2V	-5	fpBGA	900	Com	100
LFE2M100SE-6F900C	416	1.2V	-6	fpBGA	900	Com	100
LFE2M100SE-7F900C	416	1.2V	-7	fpBGA	900	Com	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484I	304	1.2V	-5	fpBGA	484	Ind	20
LFE2M20SE-6F484I	304	1.2V	-6	fpBGA	484	Ind	20
LFE2M20SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	20
LFE2M20SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672I	410	1.2V	-5	fpBGA	672	Ind	35
LFE2M35SE-6F672I	410	1.2V	-6	fpBGA	672	Ind	35
LFE2M35SE-5F484I	303	1.2V	-5	fpBGA	484	Ind	35
LFE2M35SE-6F484I	303	1.2V	-6	fpBGA	484	Ind	35
LFE2M35SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	35
LFE2M35SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900I	410	1.2V	-5	fpBGA	900	Ind	50
LFE2M50SE-6F900I	410	1.2V	-6	fpBGA	900	Ind	50
LFE2M50SE-5F672I	372	1.2V	-5	fpBGA	672	Ind	50
LFE2M50SE-6F672I	372	1.2V	-6	fpBGA	672	Ind	50
LFE2M50SE-5F484I	270	1.2V	-5	fpBGA	484	Ind	50
LFE2M50SE-6F484I	270	1.2V	-6	fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152I	430	1.2V	-5	fpBGA	1152	Ind	70
LFE2M70SE-6F1152I	430	1.2V	-6	fpBGA	1152	Ind	70
LFE2M70SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	70
LFE2M70SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1156I	616	1.2V	-5	fpBGA	1156	Ind	100
LFE2M100SE-6F1156I	616	1.2V	-6	fpBGA	1156	Ind	100
LFE2M100SE-5F1152I	520	1.2V	-5	fpBGA	1152	Ind	100
LFE2M100SE-6F1152I	520	1.2V	-6	fpBGA	1152	Ind	100
LFE2M100SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	100
LFE2M100SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2M20SE-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2M20SE-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2M20SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2M20SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2M20SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2M35SE-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2M35SE-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	Com	35
LFE2M35SE-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2M35SE-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2M35SE-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2M35SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	35
LFE2M35SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	35
LFE2M35SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	Com	50
LFE2M50SE-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	Com	50
LFE2M50SE-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	Com	50
LFE2M50SE-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2M50SE-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2M50SE-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	Com	50
LFE2M50SE-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2M50SE-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2M50SE-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152C	430	1.2V	-5	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-6FN1152C	430	1.2V	-6	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-7FN1152C	430	1.2V	-7	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2M70SE-6FN900C	416	416	-6	Lead-Free fpBGA	900	Com	70
LFE2M70SE-7FN900C	416	416	-7	Lead-Free fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1156C	616	1.2V	-5	Lead-Free fpBGA	1156	Com	100
LFE2M100SE-6FN1156C	616	1.2V	-6	Lead-Free fpBGA	1156	Com	100
LFE2M100SE-7FN1156C	616	1.2V	-7	Lead-Free fpBGA	1156	Com	100
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2M20SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	35
LFE2M35SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900I	420	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-6FN900I	420	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50SE-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152I	430	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-6FN1152I	430	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1156I	616	1.2V	-5	Lead-Free fpBGA	1156	Ind	100
LFE2M100SE-6FN1156I	616	1.2V	-6	Lead-Free fpBGA	1156	Ind	100
LFE2M100SE-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

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For Further Information

A variety of technical notes for the LatticeECP2 family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP2M SERDES/PCS Usage Guide (TN1124)
- LatticeECP2/M sysIO Usage Guide (TN1102)
- LatticeECP2/M sysCLOCK PLL Design and Usage Guide (TN1103)
- LatticeECP2/M Memory Usage Guide (TN1104)
- LatticeECP2/M High-Speed I/O Interface (TN1105)
- Power Estimation and Management for LatticeECP2/M Devices (TN1106)
- LatticeECP2/M sysDSP Usage Guide (TN1107)
- LatticeECP2/M sysCONFIG Usage Guide (TN1108)
- LatticeECP2/M Configuration Encryption Usage Guide (TN1109)
- LatticeECP2/M Soft Error Detection (SED) Usage Guide (TN1113)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

LatticeECP2/M Family Data Sheet Revision History

July 2007 **Advance Data Sheet DS1006**

Date	Version	Section	Change Summary
February 2006	01.0	—	Initial release.
August 2006	01.1	Introduction	
			Updated Table 1-1 “LatticeECP2 Family Selection Guide”
		Architecture	Updated figure 2-2 “PFU Diagram”
			Updated figure 2-13 “Secondary Clock Regions ECP2-50”
			Updated figure 2-25 “PIC Diagram”
			Updated figure 2-26 “Input Register Block for Left, Right and Bottom Edges”
			Updated figure 2-28 “Output Register Block for Left, Right and Bottom Edges”
			Updated figure 2-30 “DQS Input Routing for Left and Right Edges”
			Updated figure 2-32 “Edge Clock, DLL Calibration and DQS Local Bus Distribution”
			Table 2-15 Selectable Master clock (CCLK) frequencies Removed frequencies 15,20,21,22,23,30,34,41,45,51,55,60
			Replaced “CLKINDEL” with “CLKO”
			Updated SED section
			Qualified device migration capability when using DQS banks for DDR interfaces
		DC and Switching Characteristics	Added VCCPLL to the Recommended Operating Conditions Table
			Remove Note 5 from “Hot Specifications” section
			Added note 7 & 8 to “Initialization Supply current Table
			Change Note 6 - “...down to 95MHz” to “...down to 95MHz for DDR and 133MHz for DDR2”
			New “Typical Building Block Function Performance” numbers
			New External Switching Characteristics numbers
			New Internal Switching Characteristics numbers
			New Family Timing Adders numbers
			Updated Timings for GPLLs, SPLLs and DLLs
			Added sysConfig waveforms.
			Remove HSTL15D_II from sysIO Recommended Operating Condition Table
			Updated Supply and initialization currents for ECP2-50
		Pinout Information	Added VCCPLL to the Signal Descriptions Table
			Updated Logic signal Connections tables to include 484-fpBGA for the ECP2-50.
			Added Logic signal Connections tables for ECP2-12 devices.
			Updated Pin Information Summary table to include ECP2-12.
			Updated Power Supply and NC Connections table to include ECP2-12.
			Added Note 2 to DDR Strobe (DQS) Pin Table
			Added Information on: PCI, DDR & SPI4.2 Capabilities of the device-Package combination

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table
		Ordering Information	Updated ordering part number table to include ECP2-12.
			Updated topside mark drawing
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
			Updated timing numbers to include LFE2-12E (rev A 0.08)
		Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.
		Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added “Security Series” to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	“Security Series” ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.